

DRAWING

TITLE=J16 MLB\_IG

ABBREV=DRAWING

LAST\_MODIFIED=Fri Mar 22 11:24:26 2013

DRAWING TITLE

SCHEM,MLB IG,J16

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DRAWING NUMBER

051-0164

REVISION

12.4.0

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## Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-0052	PCBA,MLB_IG,DEV,J16	DEVELOPMENT,J16_DEVEL
639-4515	PCBA,MLB_IG,J16	J16,J16_COMMON,CPU:GOOD,SSD:Y,EEEE:FF3T
639-4704	PCBA,MLB_IG,BETTER,J16	J16,J16_COMMON,CPU:BETTER,SSD:Y,EEEE:FGWY
639-4705	PCBA,MLB_IG,CTO,J16	J16,J16_COMMON,CPU:CTO,SSD:Y,EEEE:FGY0

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	MLB LABEL, 2D	EEEE_FF3T	CRITICAL	EEEE:FF3T
825-7896	1	MLB LABEL, 2D	EEEE_FGY0	CRITICAL	EEEE:FGY0
825-7896	1	MLB LABEL, 2D	EEEE_FGWY	CRITICAL	EEEE:FGWY

## BOM Groups

BOM GROUP	BOM OPTIONS
J16_COMMON	COMMON,ALTERNATE,J16_COMMON1,J16_COMMON2,J16_PROGPARTS
J16_COMMON1	XDP,SPEAKERID,TBTHV:P12V,CPUVCC:3PHASE
J16_COMMON2	VDDQ:P1V35
J16_PROGPARTS	SMC:PROG,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG
J16_DEVEL	XDP_CONN,LPCPLUS,DDRVREF_DAC,DEVEL_SENSORS,DEVEL_AUDIO
DEVEL_SENSORS	AP_ISNS:Y,HDD_IVSNS:Y,TEMPSNSDEV
J16_PRODUCTION	AP_ISNS:N,HDD_IVSNS:N

ADD 'J16\_PRODUCTION' AT REVA RELEASE

## CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4515	1	CRM,QU2U,EU2,C0,2,7G,65W,4+3,1.15,4M,BGA	U0500	CRITICAL	CPU:GOOD
337S4516	1	CRM,QU2U,EU2,C0,3,0G,65W,4+3,1.13,4M,BGA	U0500	CRITICAL	CPU:BETTER
337S4517	1	CRM,QU2U,EU2,C0,3,2G,65W,4+3,1.3,6M,BGA	U0500	CRITICAL	CPU:CTO

## ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4483	1	LYNX POINT MOBILE,C1,Q5,QK9,FCBG4695	U1100	CRITICAL	
338S1113	1	IC,TWT,CR-48,B1,PWQ,CIO,288 12X12 FC-CHP	U2800	CRITICAL	
33S0616	1	IC,BCM57766A,CIV+,A0,8X8	U3900	CRITICAL	
343S3908	1	IC,L86561,LED BLKT CTLR,LLP24,B0-F	U8100	CRITICAL	

## Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3783	1	IC, EPI, V0039, J16	U5210	CRITICAL	BOOTROM: PROG
335S0807	1	IC, 64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM: BLANK
341S3781	1	IC, SMC, PROGRAMD, V2.12A30, J16	U5000	CRITICAL	SMC: PROG
338S1159	1	IC, SMC12-A3, 40MHZ/50MIPS, SCLP, FW, 1578CDA	U5000	CRITICAL	SMC: BLANK
341S3734	1	IC, EEPROM, CR, V16.2, J16	U2890	CRITICAL	T29ROM: PROG
335S0865	1	IC, EEPROM, SERIAL, 256KB, MLP8	U2890	CRITICAL	T29ROM: BLANK
341S3735	1	IC, ENET SD: ROM, NYMONYX, V1.13, D7/D71	U3990	CRITICAL	CIVROM: PROG
335S0862	1	IC, SERIAL FLASH, 2MBIT, 2.7V, REV F	U3990	CRITICAL	CIVROM: BLANK
341S3778	1	IC, CAMERA, FLASH, V7229, J16	U4202	CRITICAL	CAMROM: PROG
335S0852	1	IC, FLASH, SPI, 1MBIT, 3V3	U4202	CRITICAL	CAMROM: BLANK

Schematic / PCB #'s


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0164	1	SCH,MLB_IG,J16	SCH	CRITICAL	J16
820-3588	1	PCBF,MLB_IG,J16	PCB	CRITICAL	J16

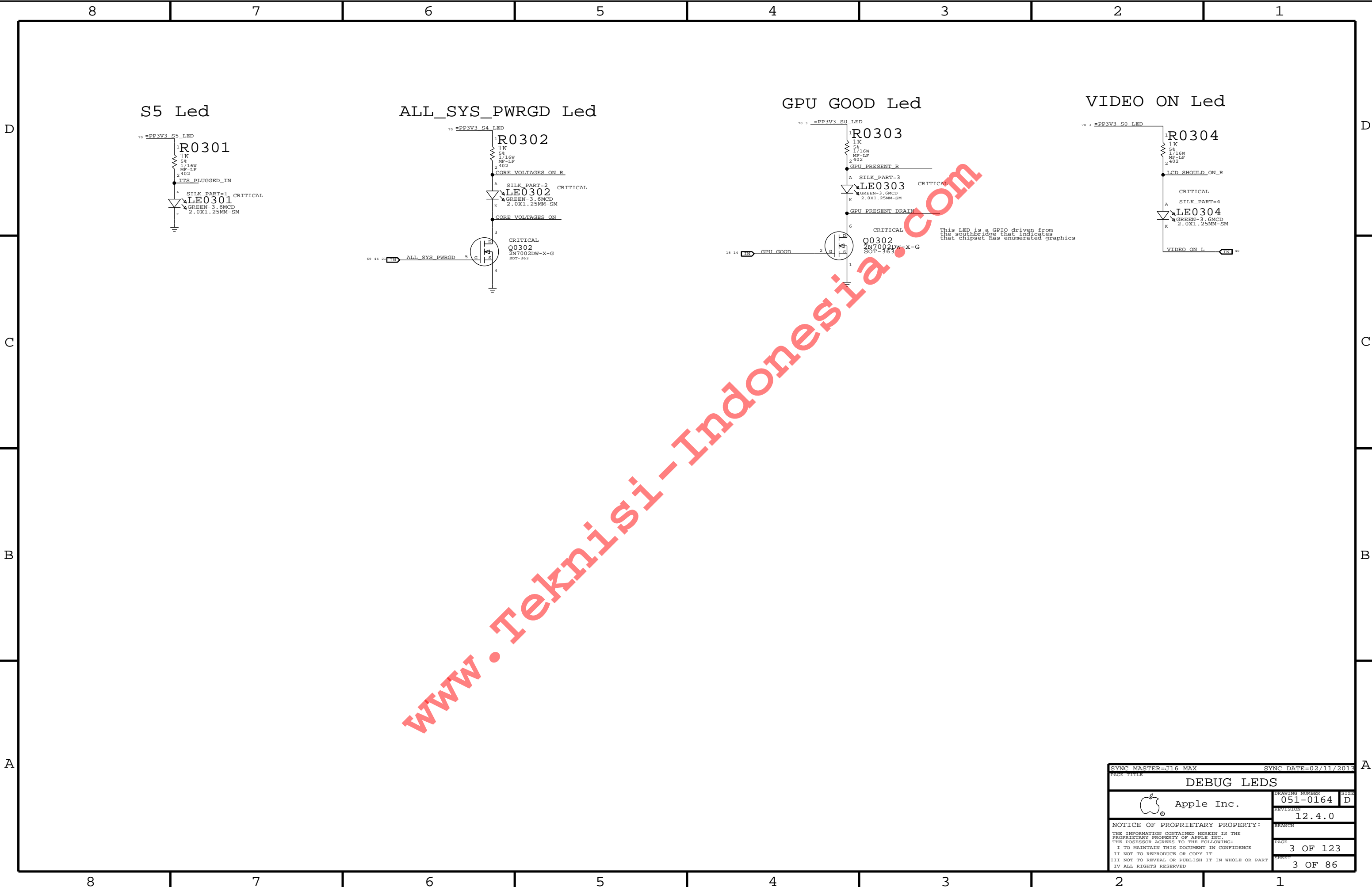
## Alternates


PART NUMBER	ALTERNATE FOR PART NUMBER	ECN OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB2 diodes
377S0155	377S0104		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
376S0075	376S1081		ALL	P/Nch dual FET
157S0084	157S0058		ALL	Enet magnetics
155S0078	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 al
197S0479	197S0478		Y4200	12 MHz Cam. Xtal
341S3747	341S3735		U3990	Enet ROM
107S0251	107S0249		ALL	Sense resistor
102S0880	102S0879		ALL	Sense resistor
197S0481	197S0480		ALL	25MHZ Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
138S0706	138S0739		ALL	Single-source 1uF 201

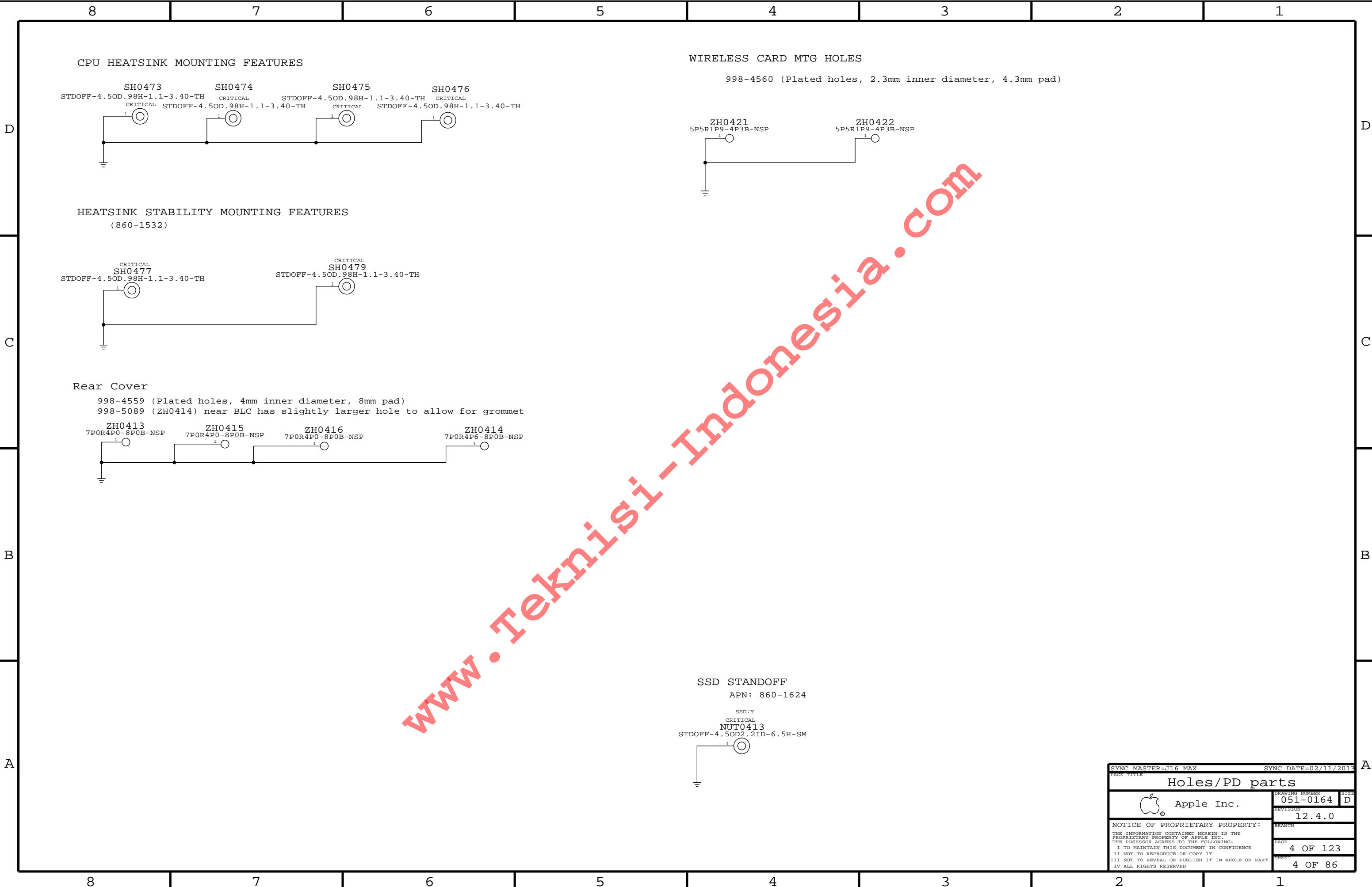
R5400, R5520, R5530


R5430

SYMC MASTER=J16 DINI		SYMC DATE=01/29/2013	
PAGE TITLE			
BOM Configuration			
	Apple Inc.		DRAWING NUMBER 051-0164
			SIZE D
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		2 OF 86	



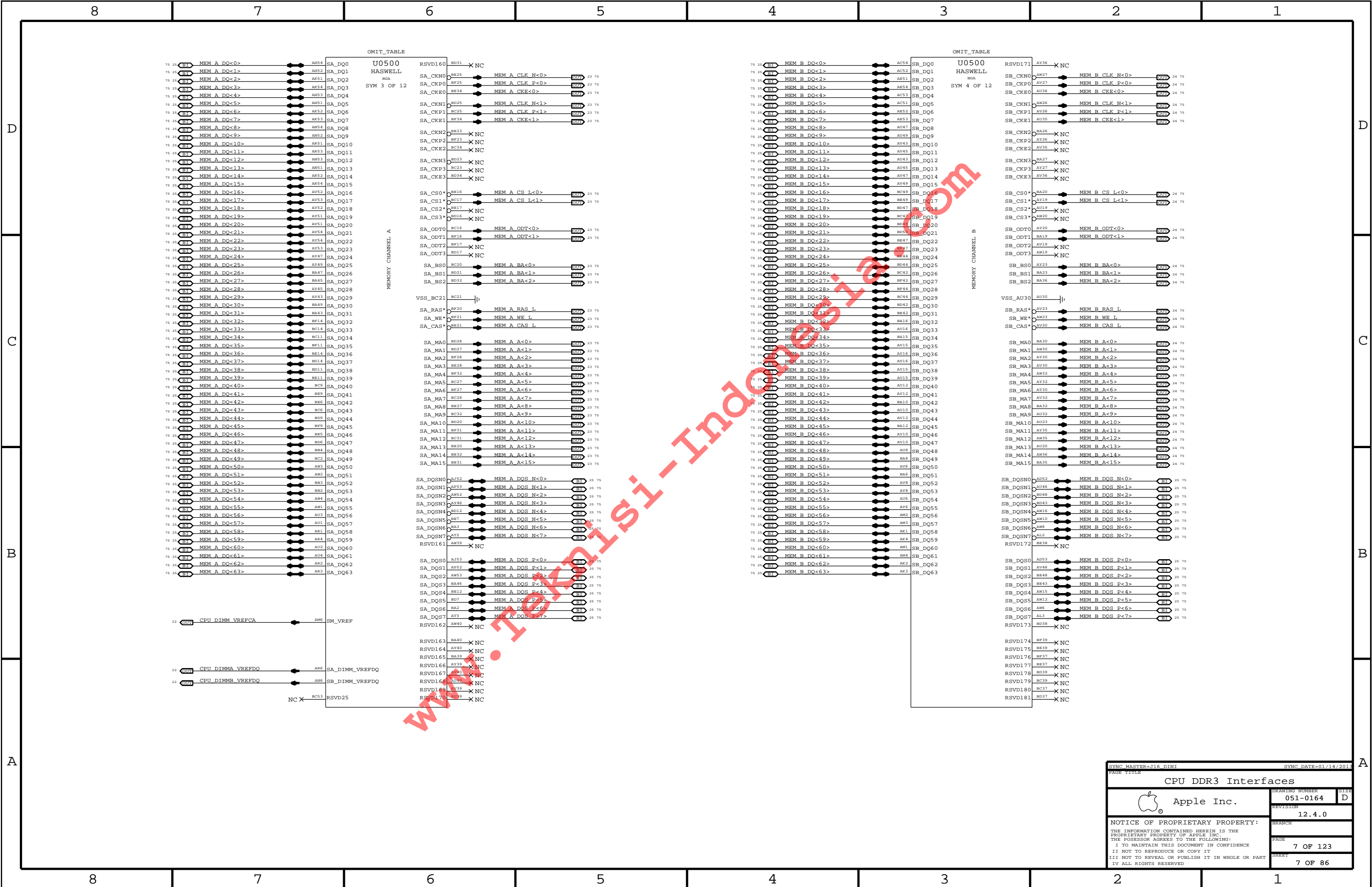
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DEBUG LEDS			
 Apple Inc.		DRAWING NUMBER	051-0164
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		PAGE	3 OF 123
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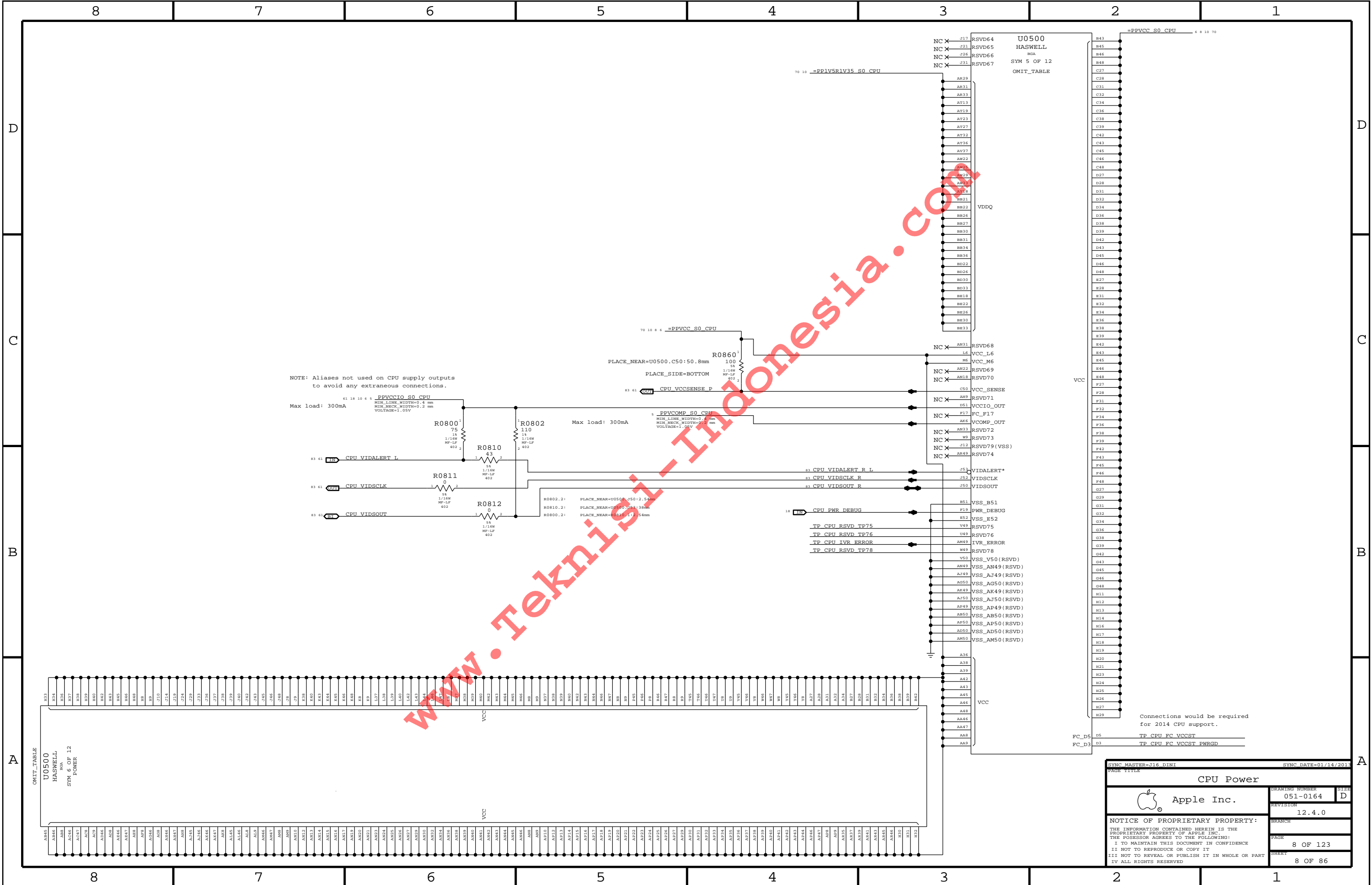


SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
PAGE TITLE			
Holes/PD parts			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-0164		D
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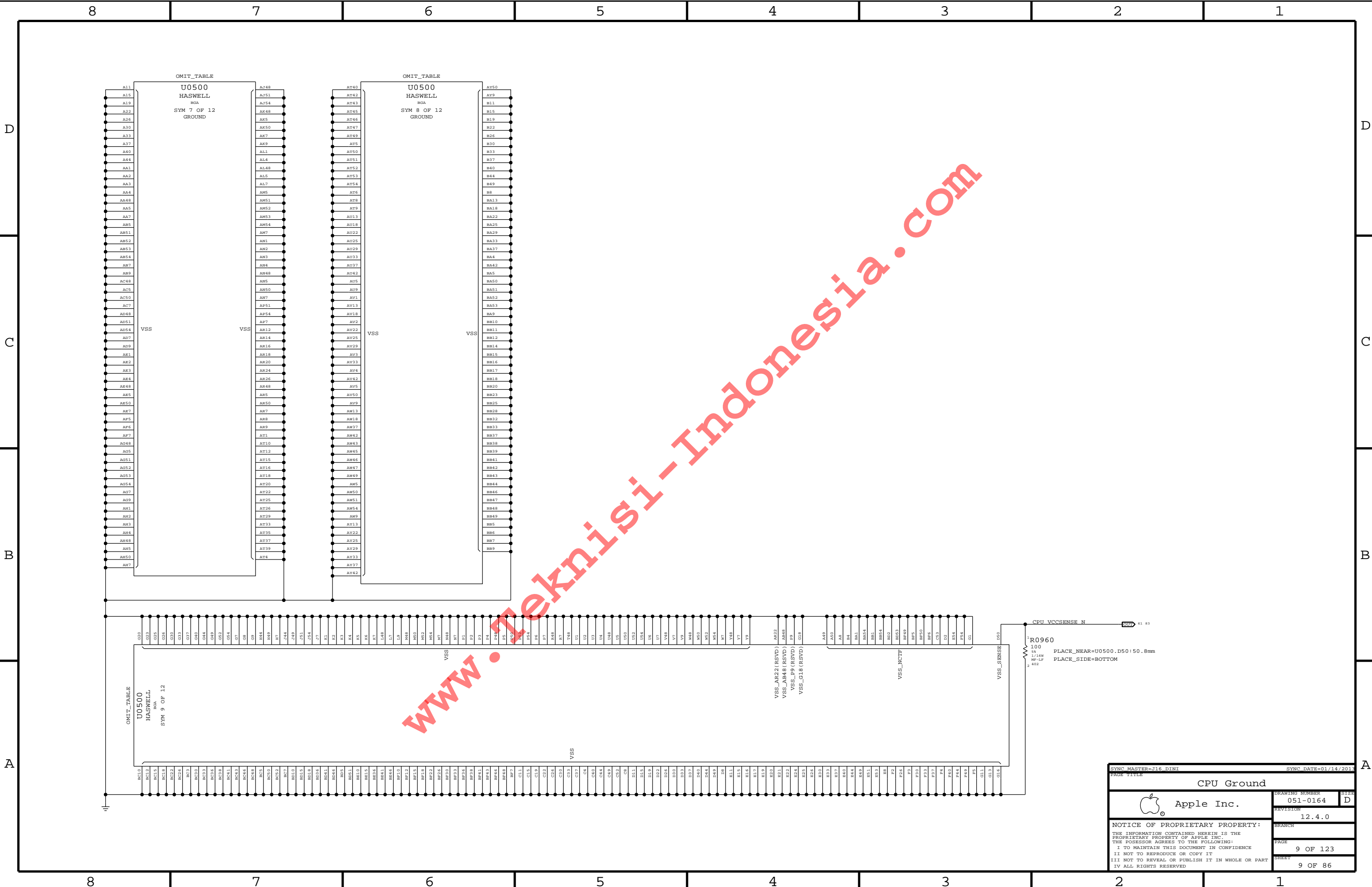


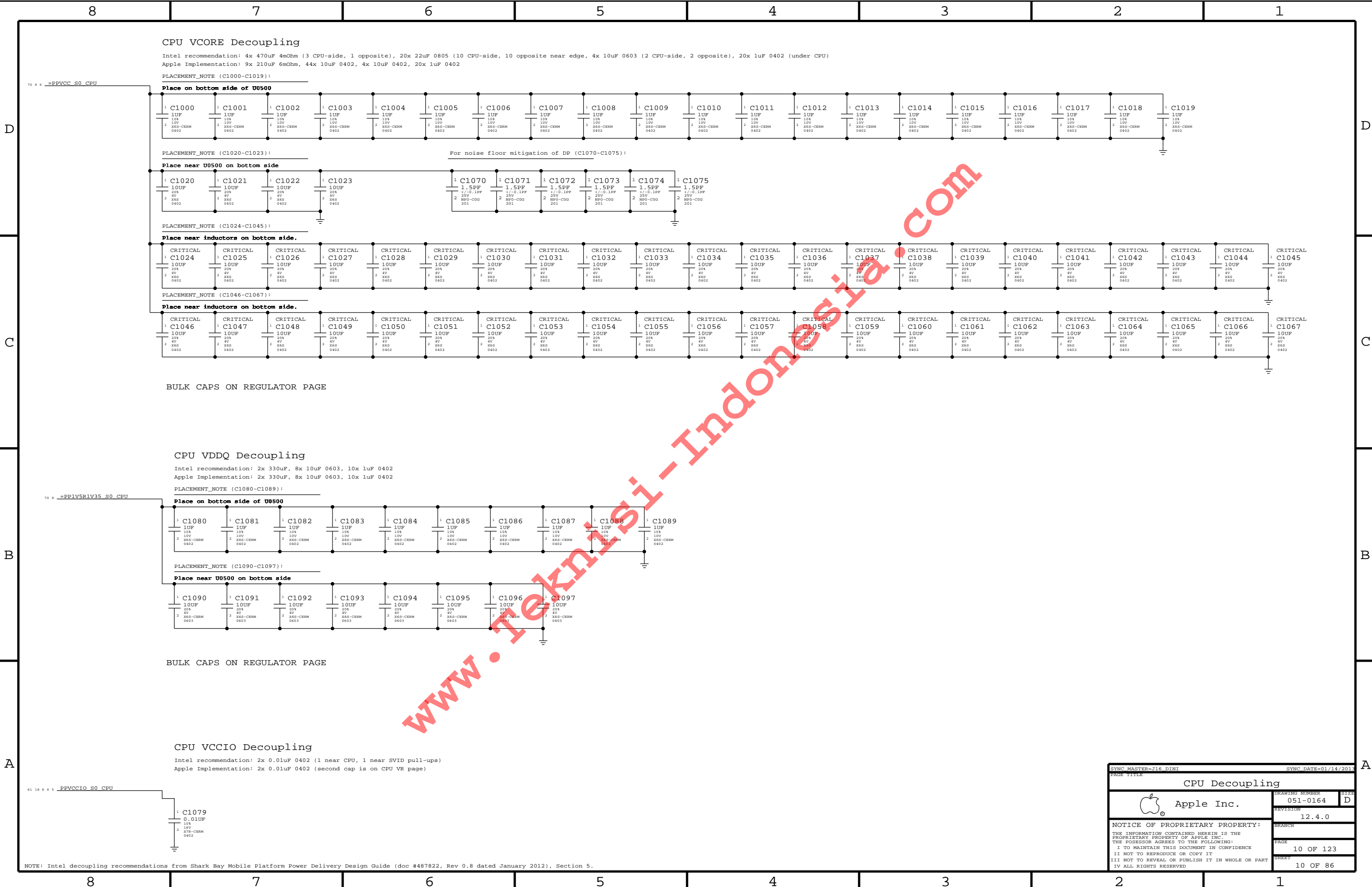





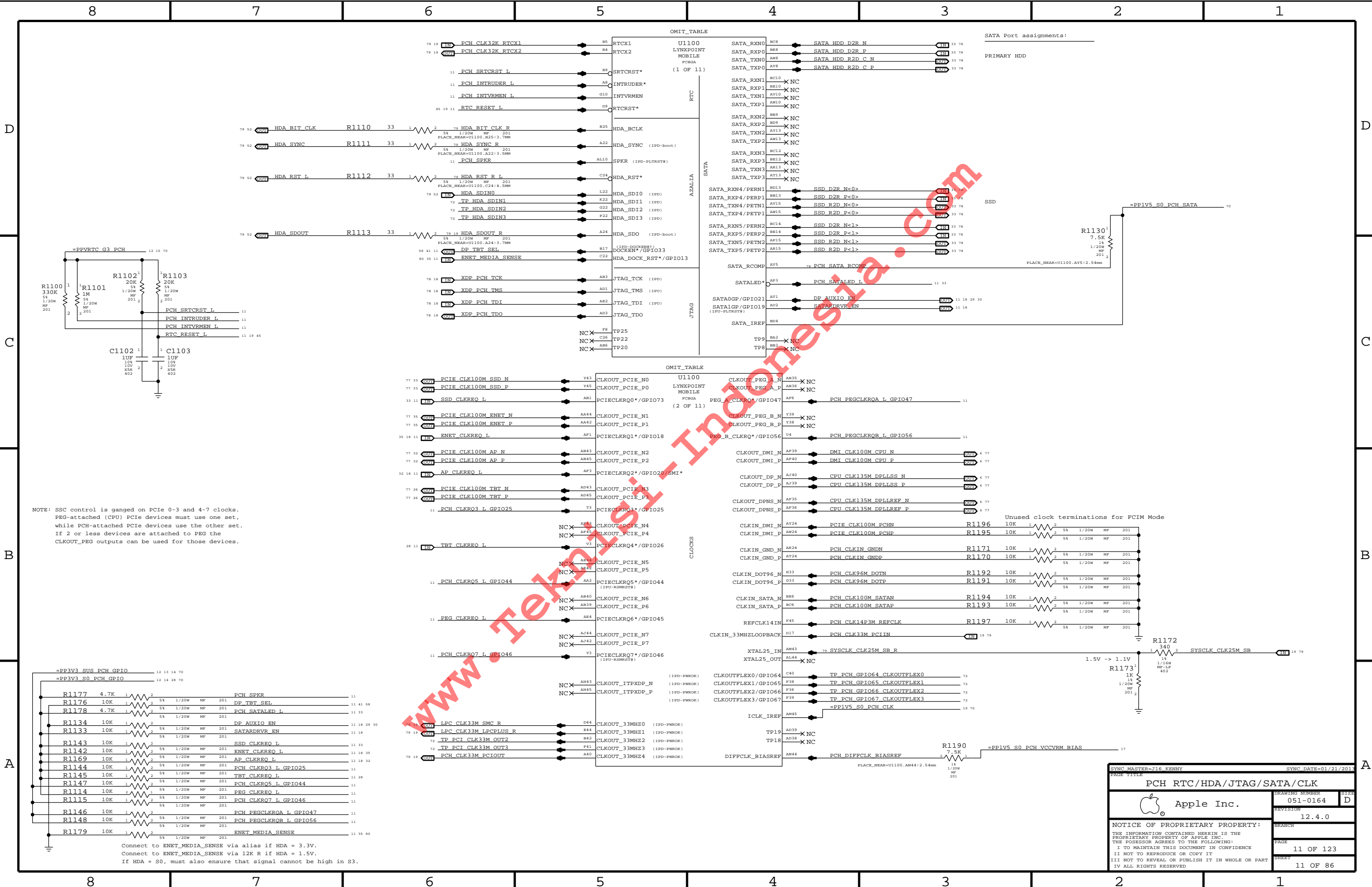


SYNC MASTER=J16 DINI		SYNC DATE=01/14/2013	
PAGE TITLE		CPU Power	
Apple Inc.		DRAWING NUMBER	051-0164
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CPU Decoupling			
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NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.  
PEG-attached (CPU) PCIe devices must use one set,  
while PCH-attached PCIe devices use the other set.  
If 2 or less devices are attached to PEG the  
CLKOUT\_PEG outputs can be used for those devices.

SYNC MASTER=J16 KENNY

SYNC DATE=01/21/2013

PAGE TITLE

PCH RTC/HDA/JTAG/SATA/CLK

Apple Inc.

D

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051-0164

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PAGE

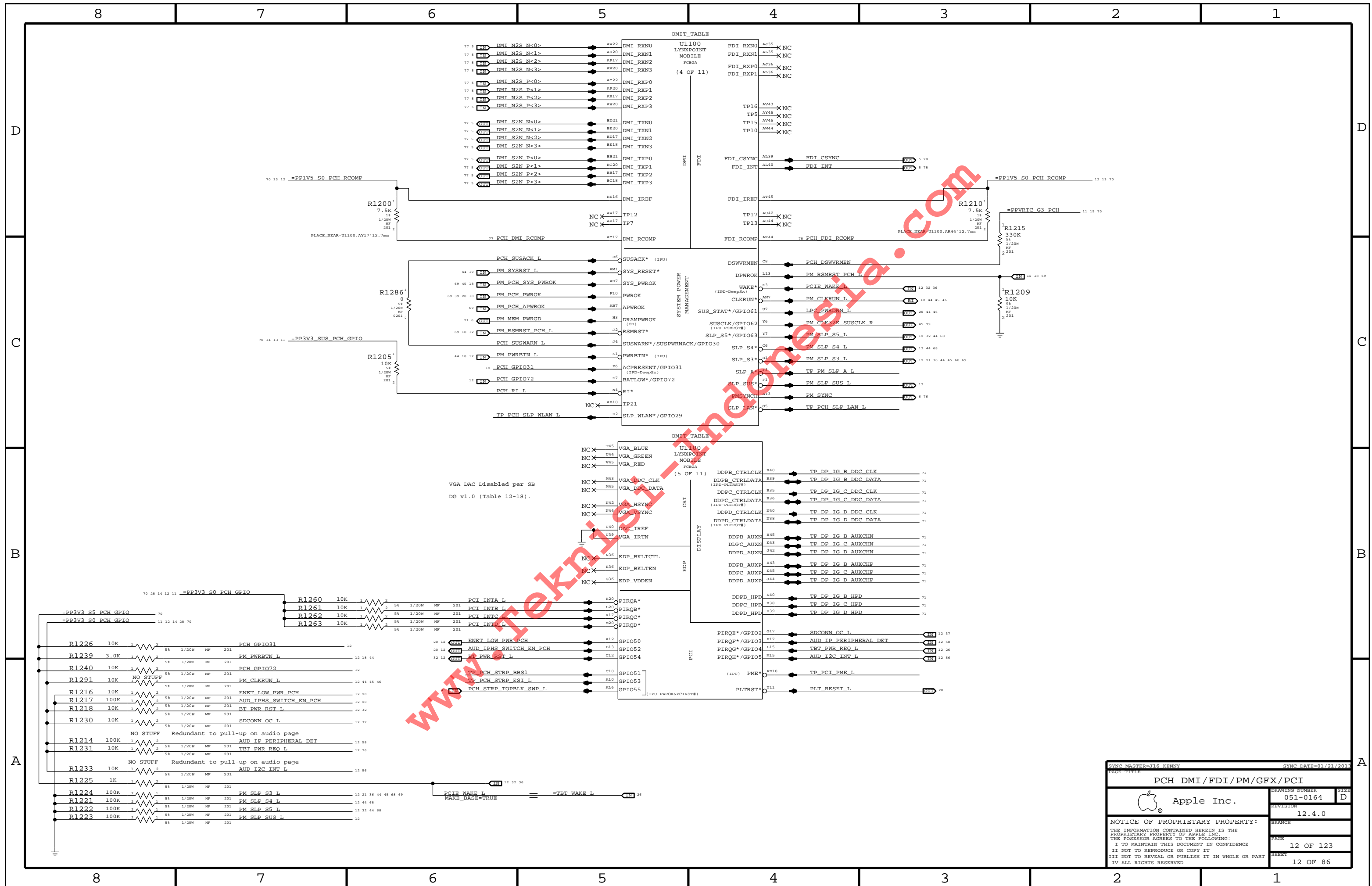
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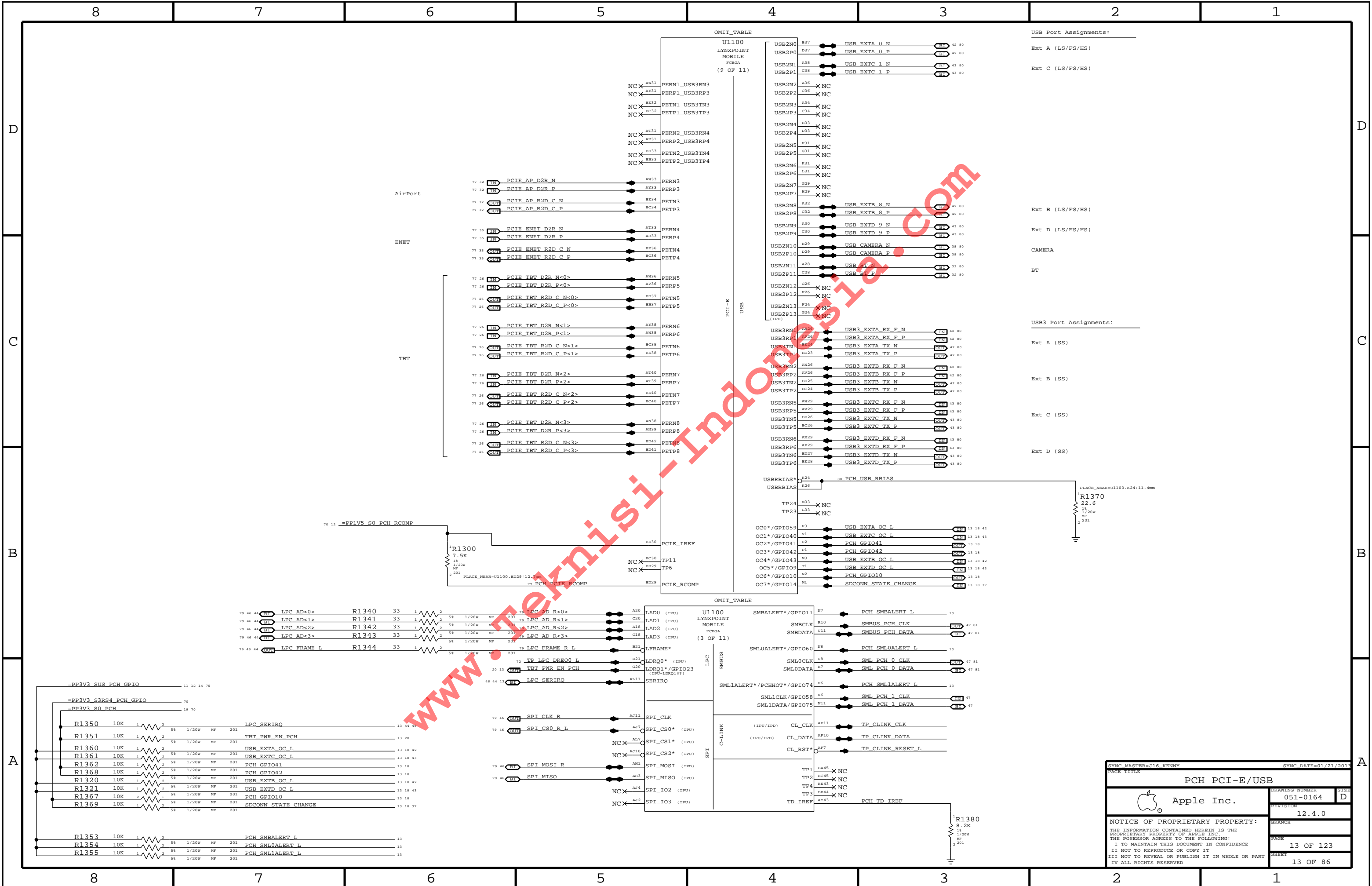
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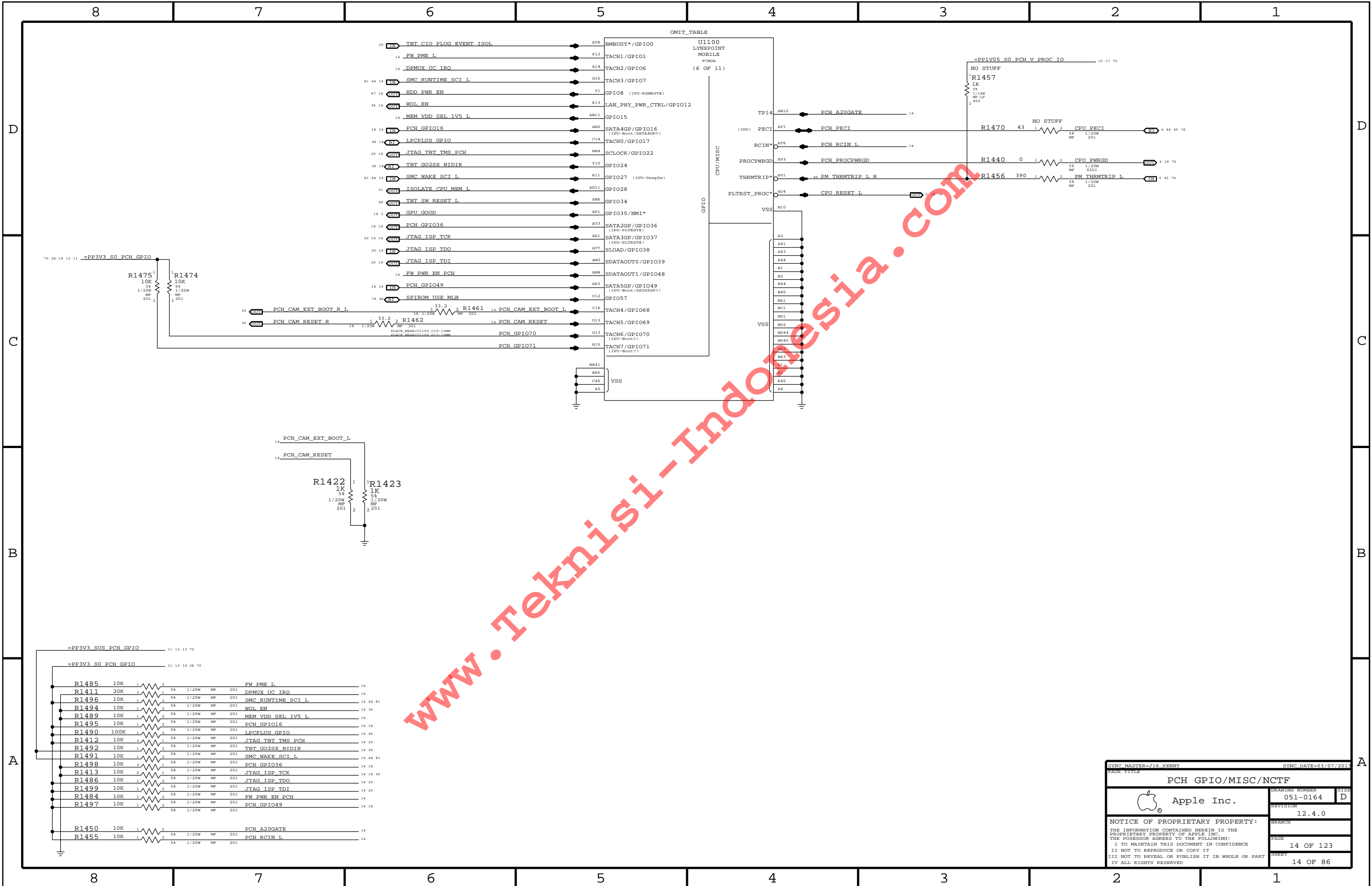
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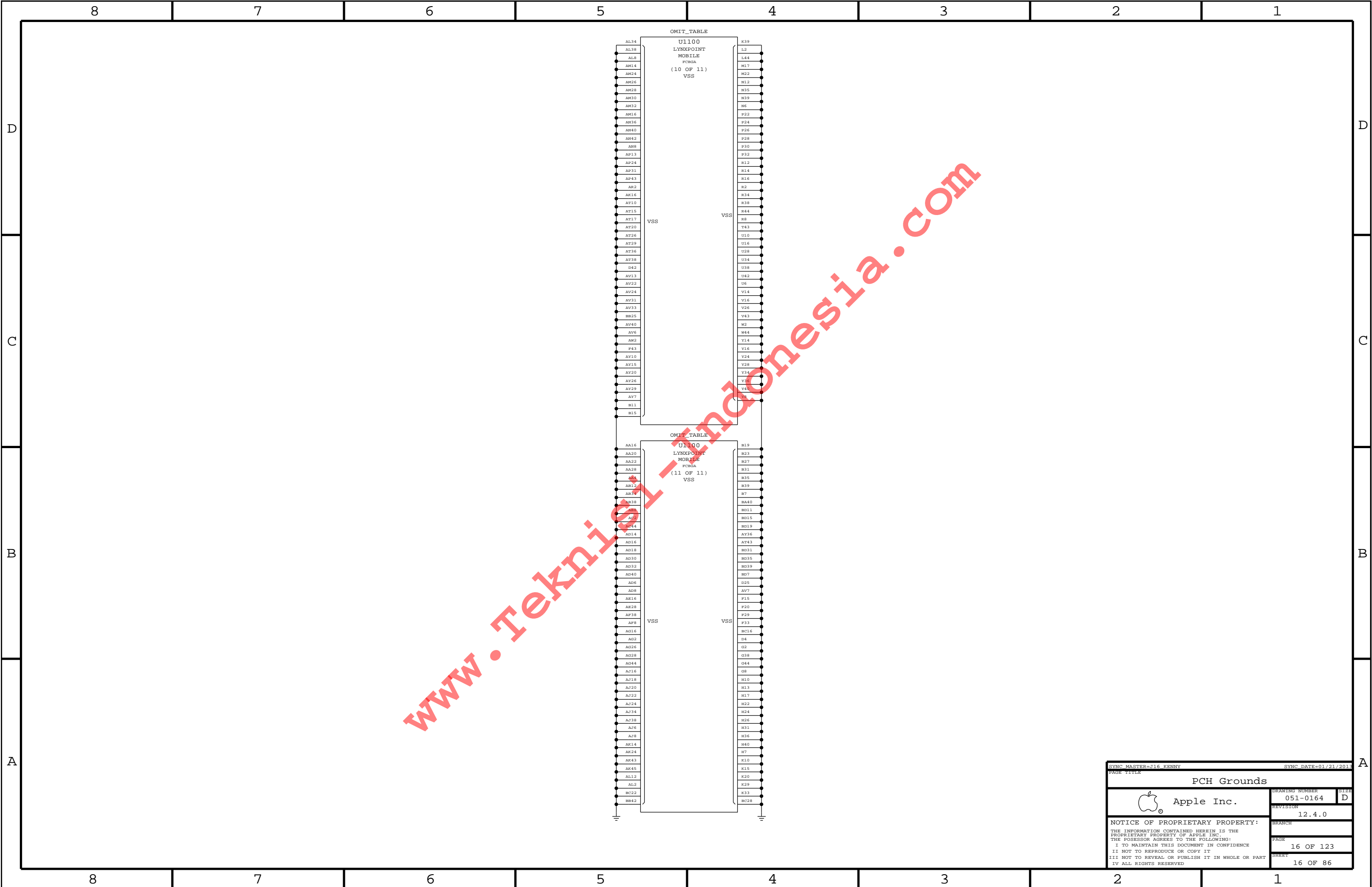
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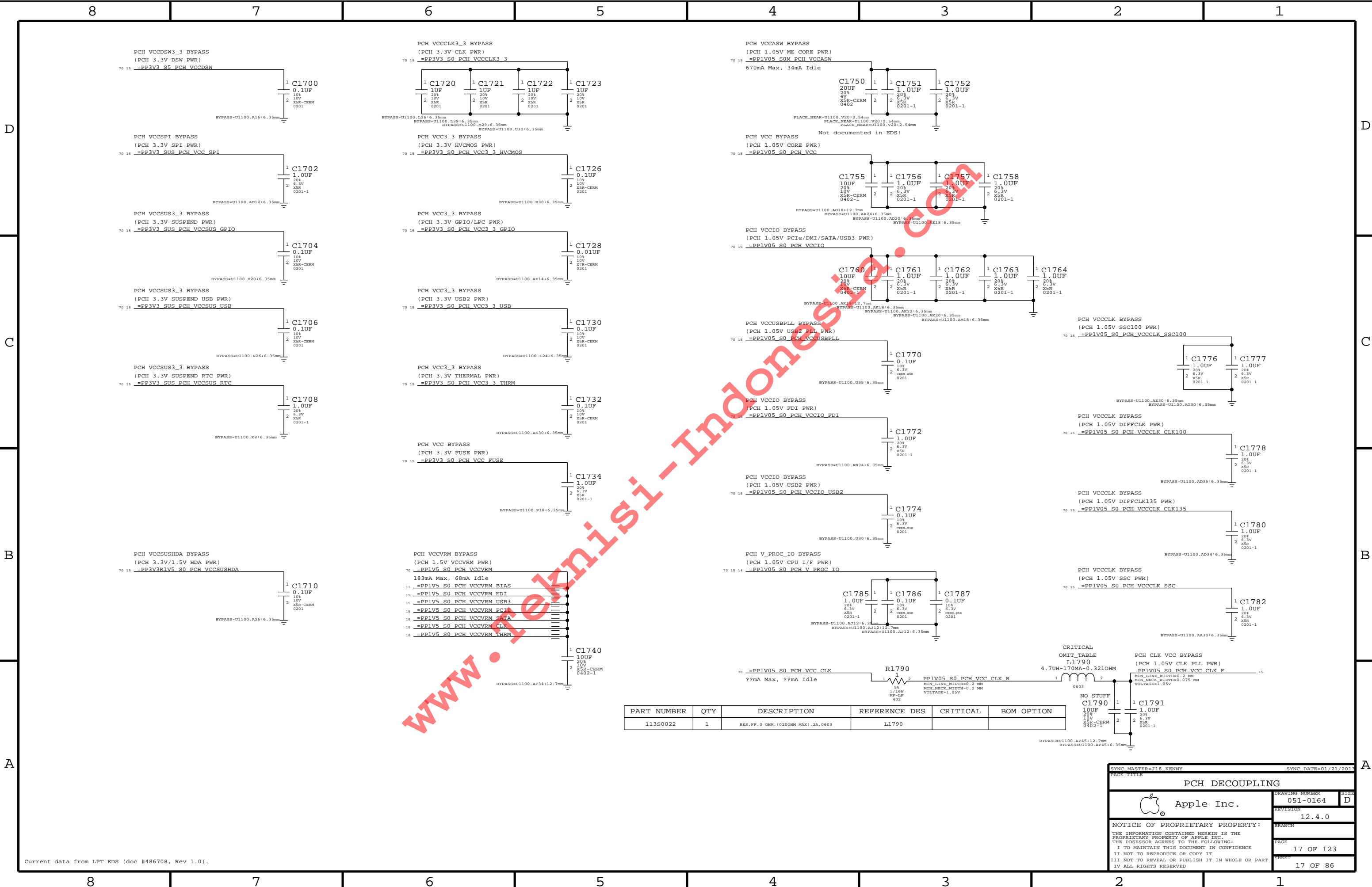




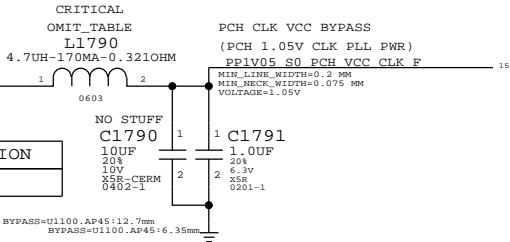





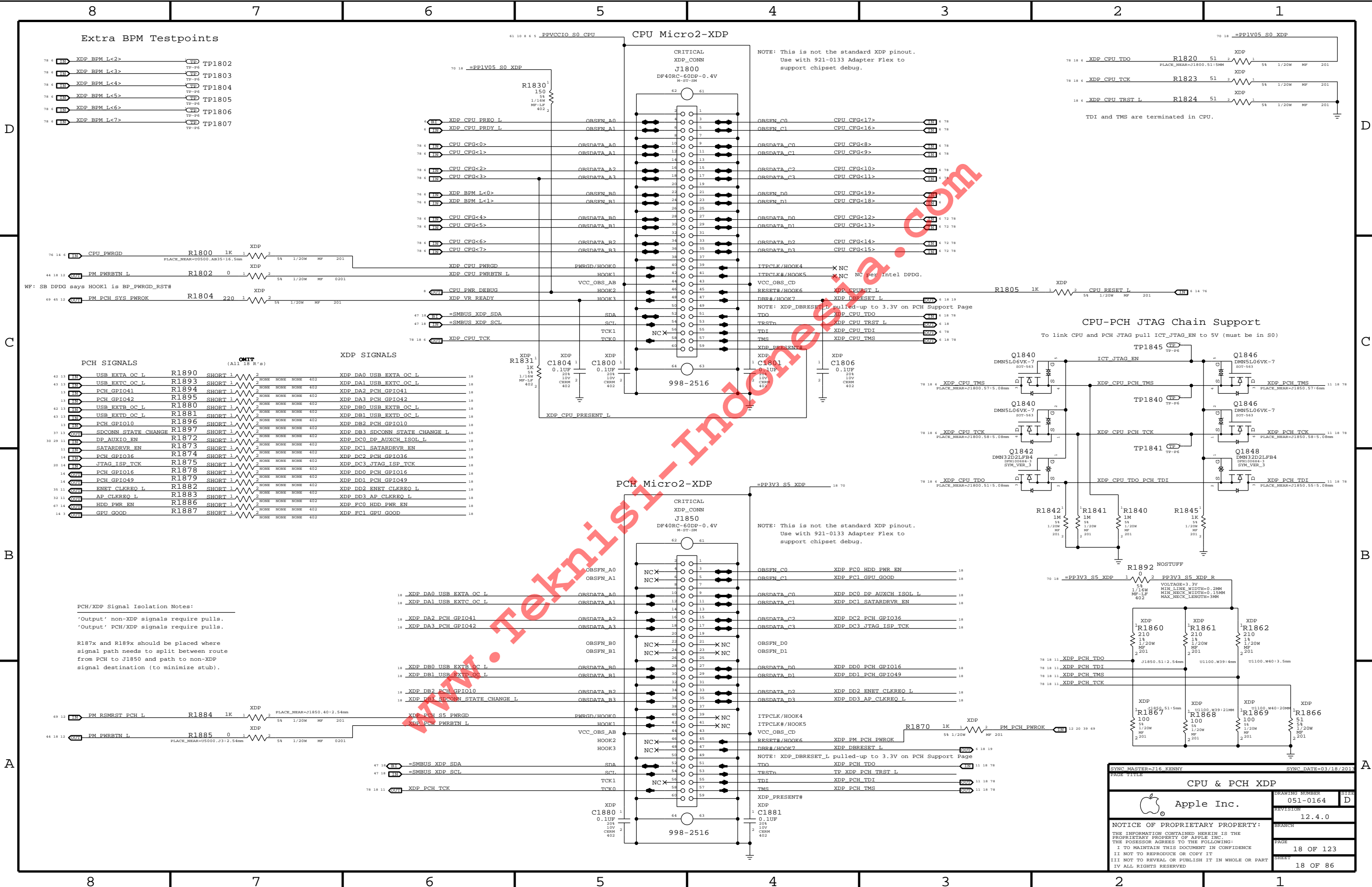




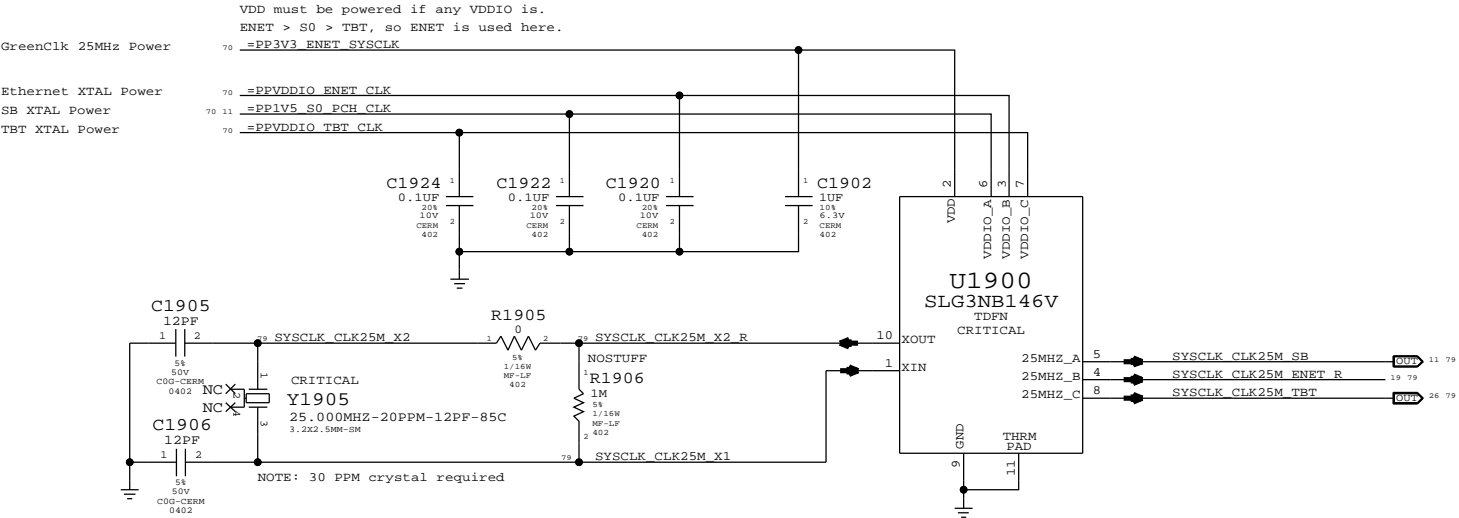
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FP,0 OHM,(020OHM MAX),2a,0603	L1790		



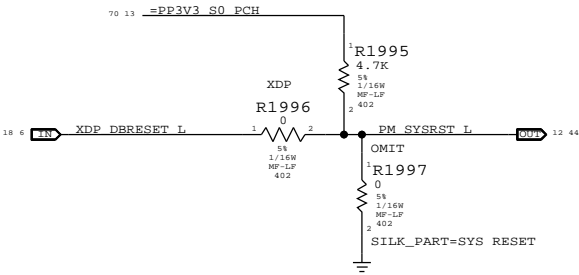
SYNC MASTER=J16 KENNY		SYNC DATE=01/21/2013	
PAGE TITLE			
PCH DECOUPLING			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE D
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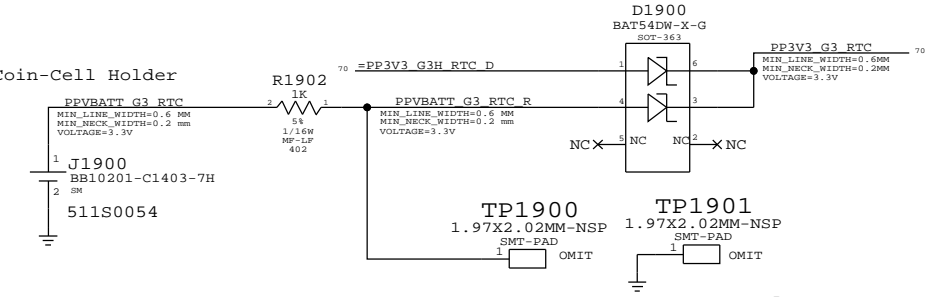
System 25MHz Clock Generator



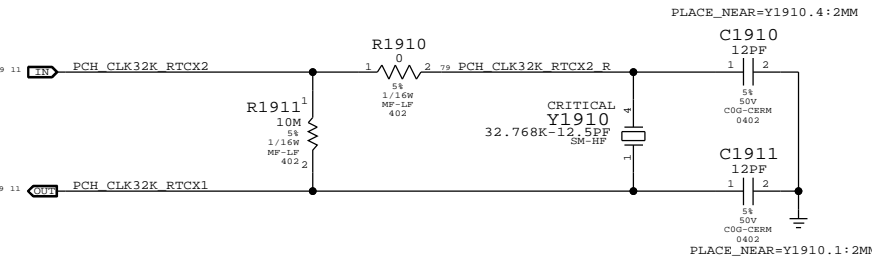
PCH Reset Button



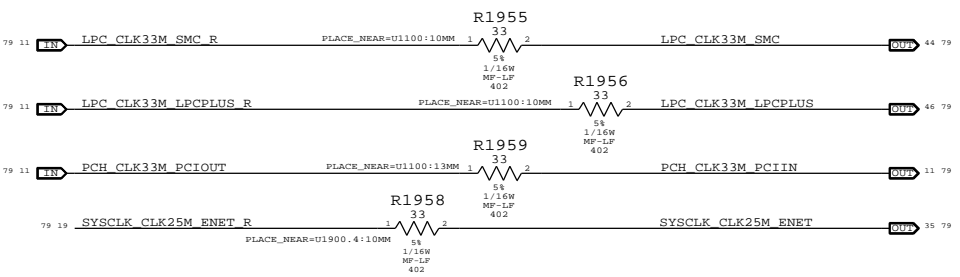
RTC Power Sources



PCH RTC Crystal

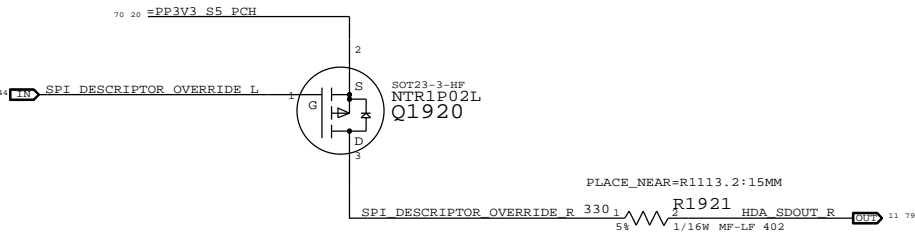



Clock series termination

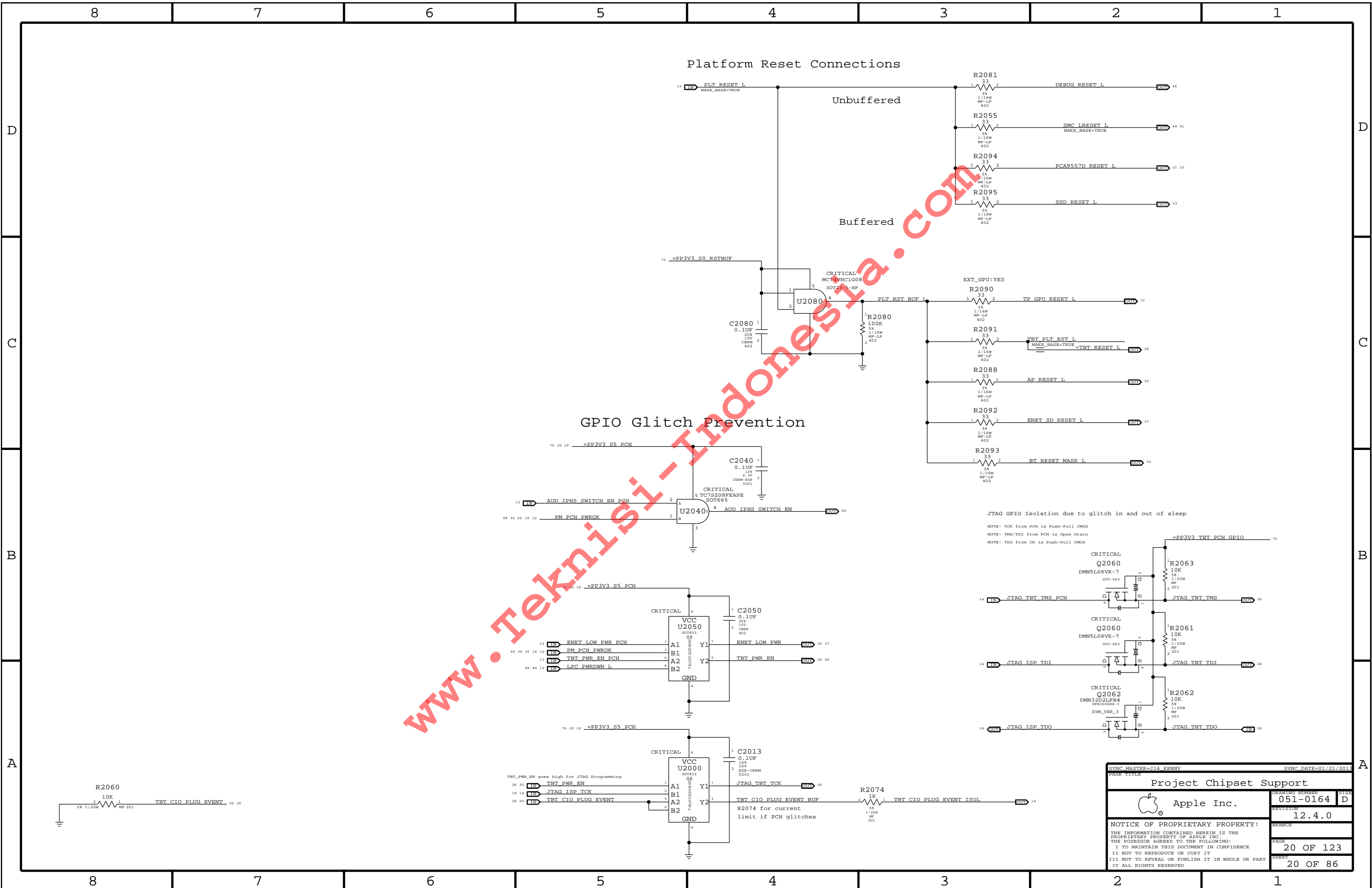


PCH ME Disable Strap

PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting.



SYNC MASTER=J16 KENNY		SYNC DATE=01/21/2013	
PAGE TITLE			
Chipset Support			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE D
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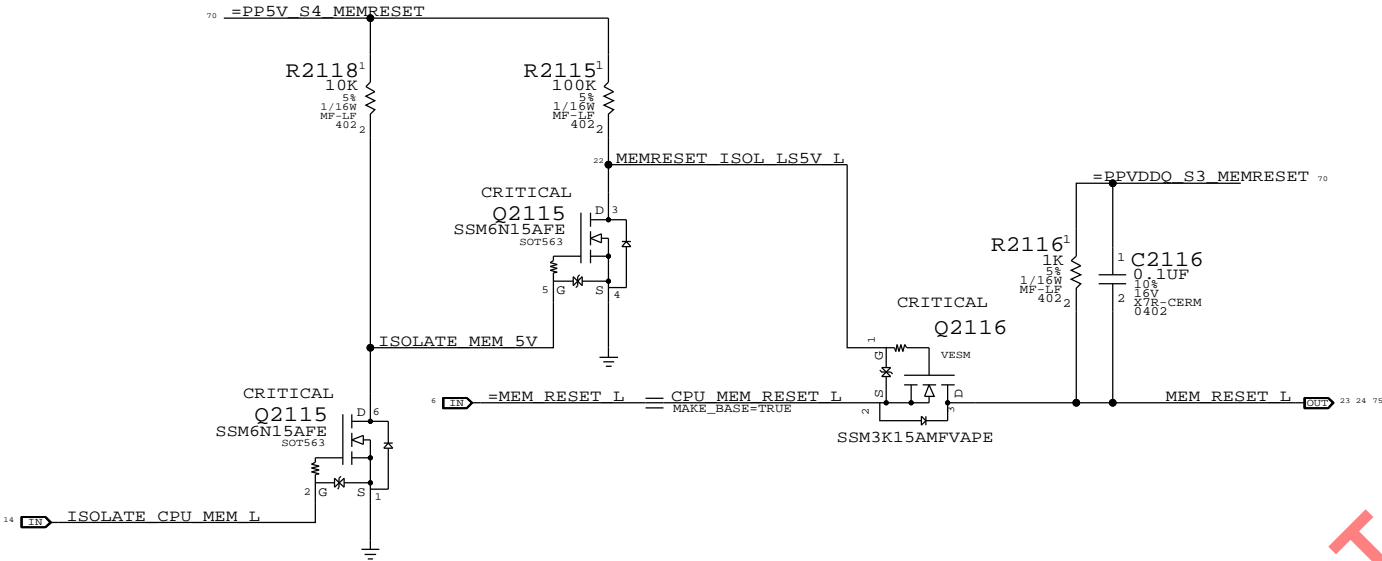
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3<->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

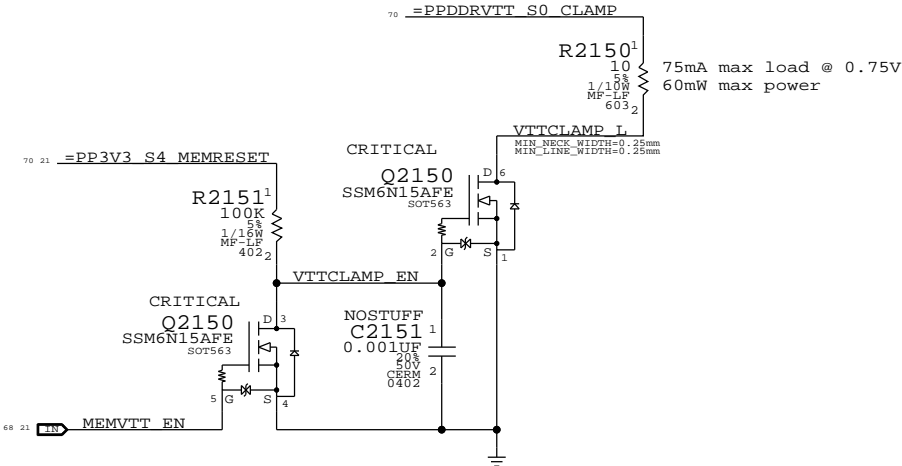
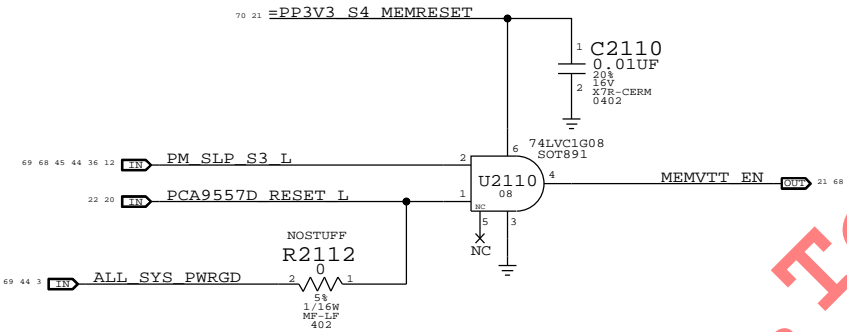
```
MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```



PM\_MEM\_PWRGD pull-up to CPU VTT rail is on CPU page  
PM\_MEM\_PWRGD MUST ASSERT MIN 100 NS AFTER MEM\_VDDQ RAMPs 80%  
THIS IS GUARANTEED BY THE 2 V/MS RAMP RATE OF THE FET

MEMVTT Clamp

Ensures CKE signals are held low in S3

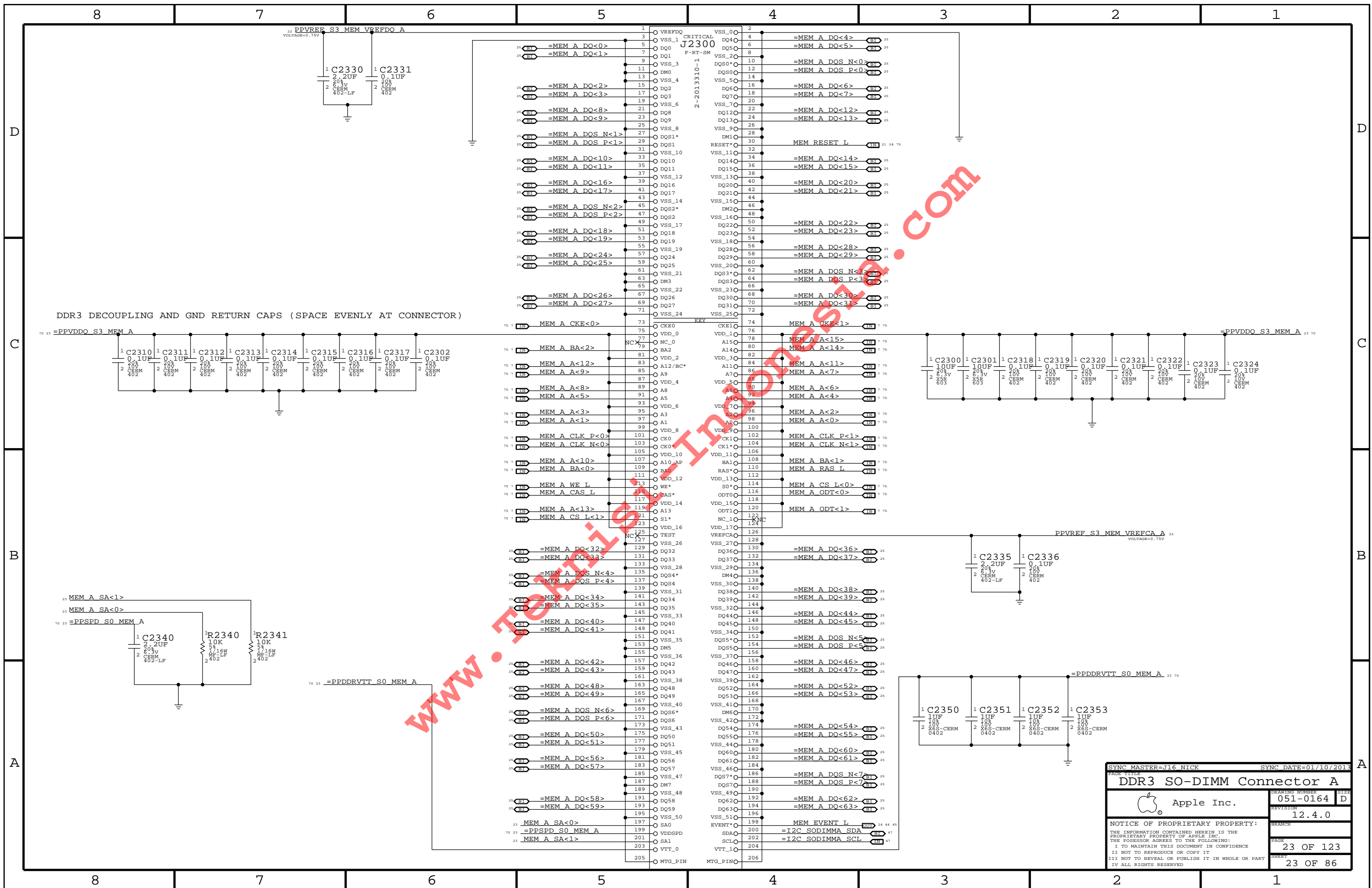


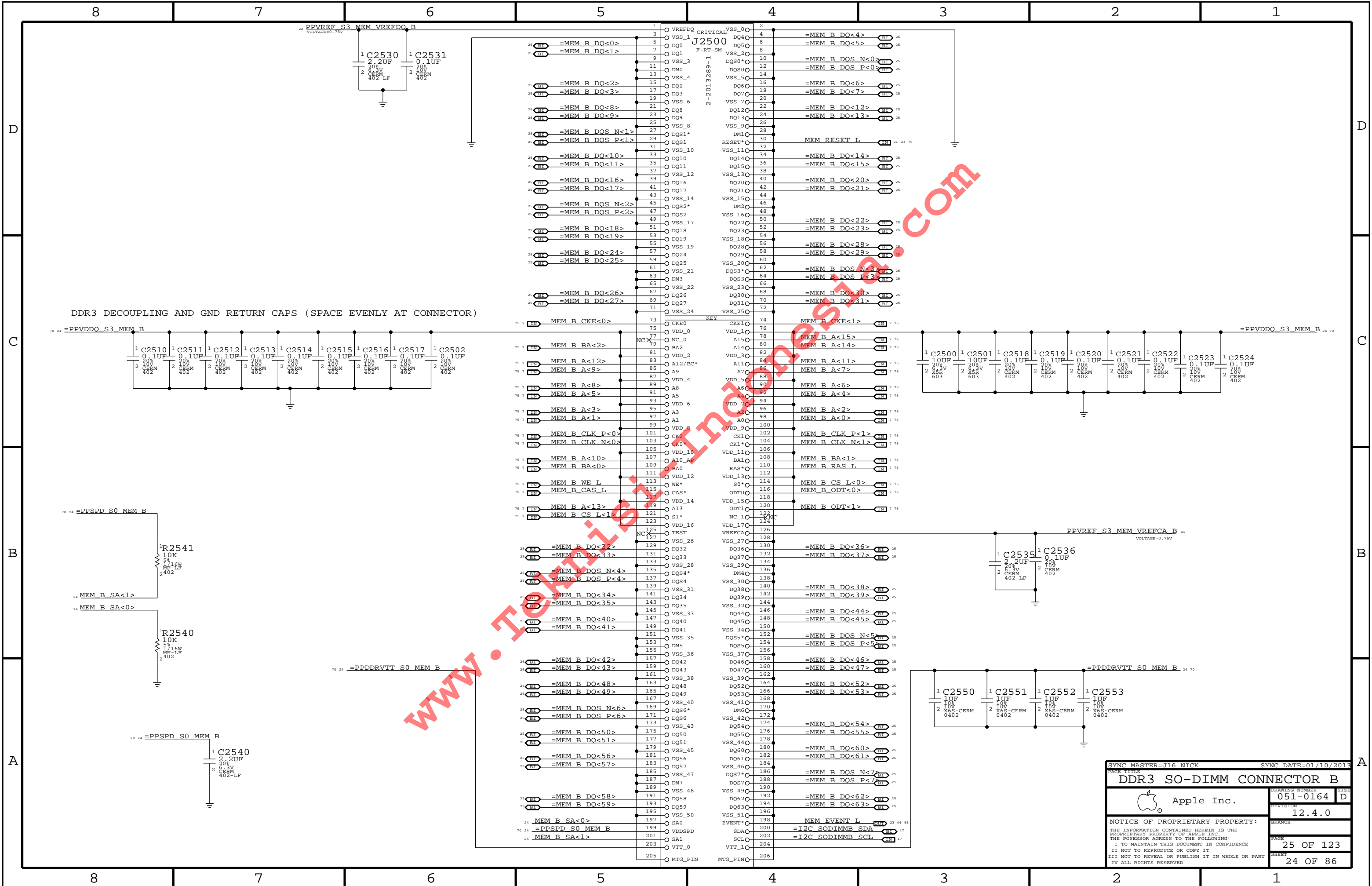
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1
2	0	0	1	1	1	0
3	0	0	0	X	1	0
4	0	0	1	X	1	0
5	0	1	1	0 (*)	1	1
6	0	1	1	1	1	1
S0	7	1	1	1	CPU_MEM_RESET_L	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must de-assert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.







PAGE TITLE		SYNC DATE=01/10/2013	
DDR3 SO-DIMM CONNECTOR B		DRAWING NUMBER	051-0164
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8		7		6		5		4		3		2		1	
THERE ARE NO PIN SWAPS															
D	75	MEM A DQS N<0>	==	=MEM A DQS N<0>	23	75	MEM B DQS N<0>	==	=MEM B DQS N<0>	24					
	75	MEM A DQS P<0>	==	=MEM A DQS P<0>	23	75	MEM B DQS P<0>	==	=MEM B DQS P<0>	24					
	75	MEM A DQ<7>	==	=MEM A DQ<7>	23	75	MEM B DQ<7>	==	=MEM B DQ<7>	24					
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	75	MEM A DQ<2>	==	=MEM A DQ<2>	23	75	MEM B DQ<2>	==	=MEM B DQ<2>	24					
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C	75	MEM A DQS N<1>	==	=MEM A DQS N<1>	23	75	MEM B DQS N<1>	==	=MEM B DQS N<1>	24					
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	75	MEM A DQ<8>	==	=MEM A DQ<8>	23	75	MEM B DQ<8>	==	=MEM B DQ<8>	24					
B	75	MEM A DQS N<2>	==	=MEM A DQS N<2>	23	75	MEM B DQS N<2>	==	=MEM B DQS N<2>	24					
	75	MEM A DQS P<2>	==	=MEM A DQS P<2>	23	75	MEM B DQS P<2>	==	=MEM B DQS P<2>	24					
	75	MEM A DQ<23>	==	=MEM A DQ<23>	23	75	MEM B DQ<23>	==	=MEM B DQ<23>	24					
	75	MEM A DQ<22>	==	=MEM A DQ<22>	23	75	MEM B DQ<22>	==	=MEM B DQ<22>	24					
	75	MEM A DQ<21>	==	=MEM A DQ<21>	23	75	MEM B DQ<21>	==	=MEM B DQ<21>	24					
	75	MEM A DQ<20>	==	=MEM A DQ<20>	23	75	MEM B DQ<20>	==	=MEM B DQ<20>	24					
	75	MEM A DQ<19>	==	=MEM A DQ<19>	23	75	MEM B DQ<19>	==	=MEM B DQ<19>	24					
	75	MEM A DQ<18>	==	=MEM A DQ<18>	23	75	MEM B DQ<18>	==	=MEM B DQ<18>	24					
	75	MEM A DQ<17>	==	=MEM A DQ<17>	23	75	MEM B DQ<17>	==	=MEM B DQ<17>	24					
	75	MEM A DQ<16>	==	=MEM A DQ<16>	23	75	MEM B DQ<16>	==	=MEM B DQ<16>	24					
A	75	MEM A DQS N<3>	==	=MEM A DQS N<3>	23	75	MEM B DQS N<3>	==	=MEM B DQS N<3>	24					
	75	MEM A DQS P<3>	==	=MEM A DQS P<3>	23	75	MEM B DQS P<3>	==	=MEM B DQS P<3>	24					
	75	MEM A DQ<31>	==	=MEM A DQ<31>	23	75	MEM B DQ<31>	==	=MEM B DQ<31>	24					
	75	MEM A DQ<30>	==	=MEM A DQ<30>	23	75	MEM B DQ<30>	==	=MEM B DQ<30>	24					
	75	MEM A DQ<29>	==	=MEM A DQ<29>	23	75	MEM B DQ<29>	==	=MEM B DQ<29>	24					
	75	MEM A DQ<28>	==	=MEM A DQ<28>	23	75	MEM B DQ<28>	==	=MEM B DQ<28>	24					
	75	MEM A DQ<27>	==	=MEM A DQ<27>	23	75	MEM B DQ<27>	==	=MEM B DQ<27>	24					
	75	MEM A DQ<26>	==	=MEM A DQ<26>	23	75	MEM B DQ<26>	==	=MEM B DQ<26>	24					
	75	MEM A DQ<25>	==	=MEM A DQ<25>	23	75	MEM B DQ<25>	==	=MEM B DQ<25>	24					
	75	MEM A DQ<24>	==	=MEM A DQ<24>	23	75	MEM B DQ<24>	==	=MEM B DQ<24>	24					
Sync Master=J16 Nick      Sync Date=01/10/2013															
DDR3 ALIASES AND BITSWAPS															
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SYNC MASTER=J16 NICK

SYNC DATE=01/10/2013

PAGE TITLE

DDR3 ALIASES AND BITSWAPS

 Apple Inc.

DRAWING NUMBER  
051-0164

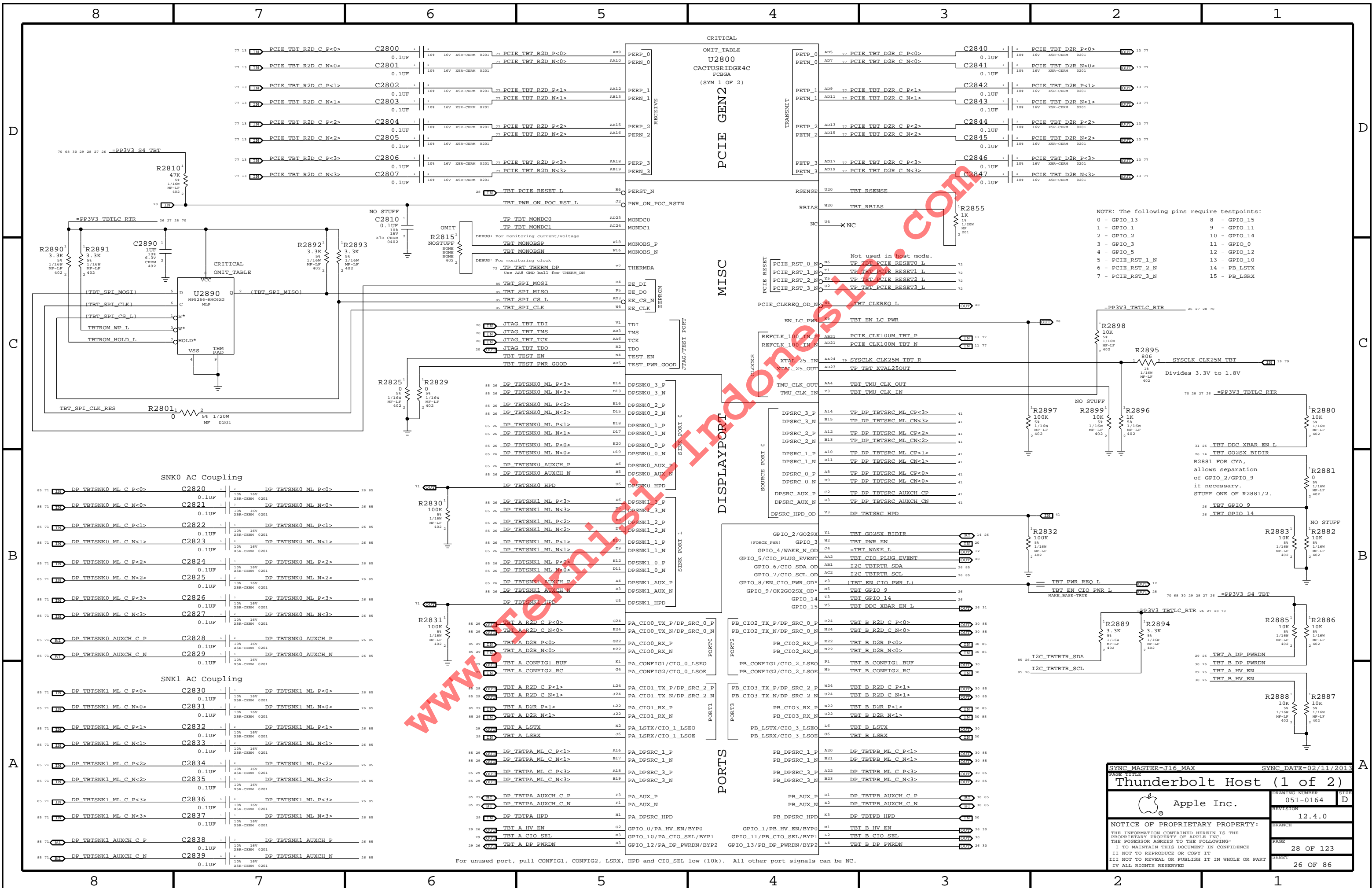
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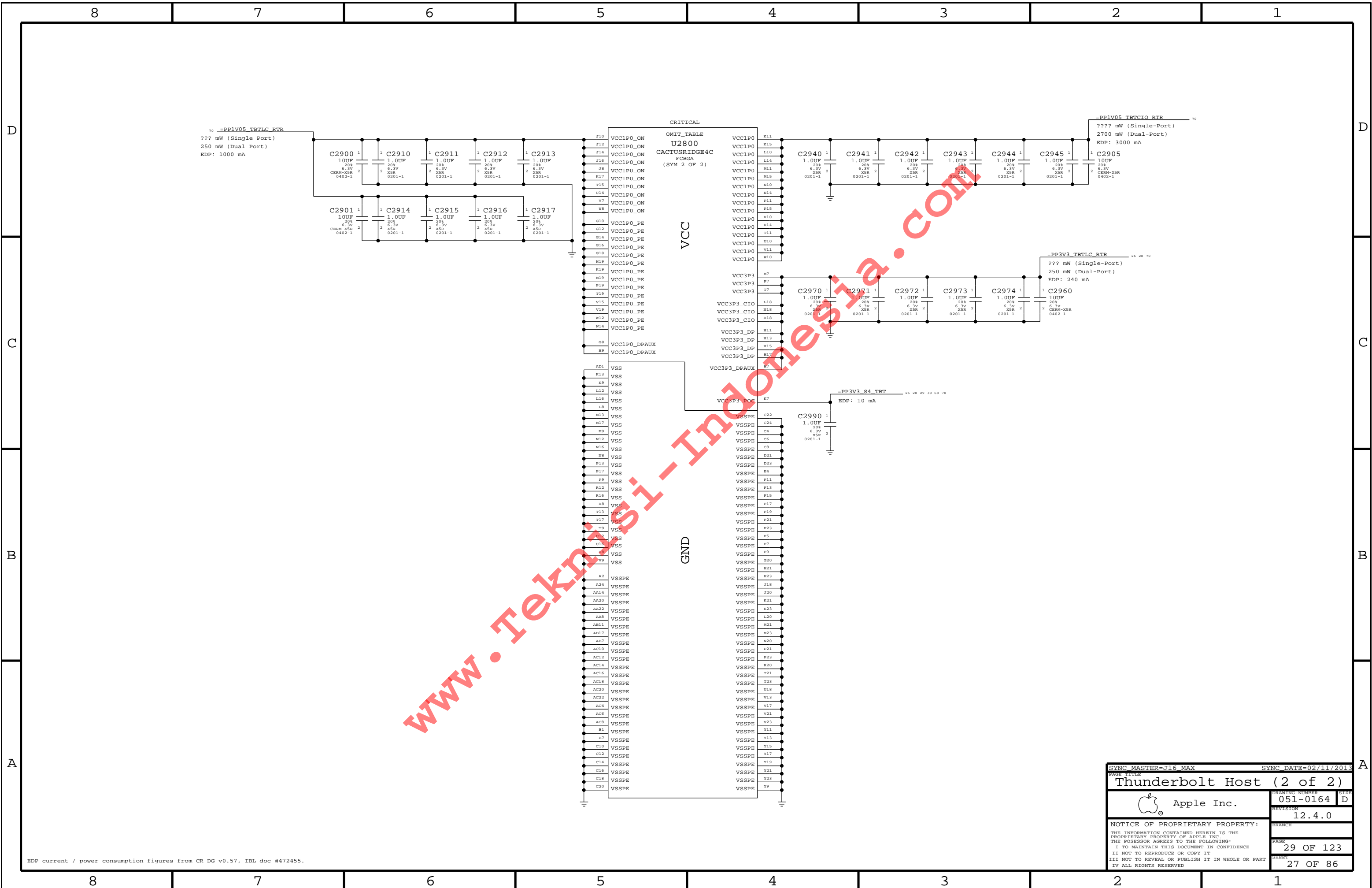
SHEET  
25 OF 86




NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
PAGE TITLE			
Thunderbolt Host (1 of 2)			
Apple Inc.		DRAWING NUMBER	051-0164
REVISION		12.4.0	SIZE
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EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013		
PAGE TITLE				
Thunderbolt Host (2 of 2)		DRAWING NUMBER	051-0164	
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		SHEET	27 OF 86	
		SIZE		D

```

Power aliases required by this page:
- =PPVIN_SW_TBTBST      (8-13V Boost Input)
- =PP15V_TBT_REG        (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFFET (3.3V FET Input)
- =PP3V3_TBT_FET        (3.3V FET Output)
- =PP3V3_S0_TBTBPRCTL
- =PP1V05_TBT_P1V05TBTFFET (1.05V FET Input)
- =PP1V05_TBT_FET        (1.05V FET Output)

```

---

```

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

```

---

```

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

```

[illegible]

70 =PP3V3\_S0\_P3V3TBTFTET

70 =PP3V3\_TBTLC\_FET

Max Current = 2A (85C)

U3010

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

1.05V TBT "LC" Switch

70 =PP1V05\_S0\_P1V05TBTFTET


70 =PP1V05\_TBTLC\_FET

Max Current = 2A (85C)

U3015

Part	TPS22924C
Type	Load Switch
R(on)	20.3 mOhm Typ
@ 1.0V	28.6 mOhm Max

[illegible][illegible]

SYNC MASTER=J16 MAX		SYNC DATE=02/11/2013	
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Thunderbolt Power Support			
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		REVISION 12.4.0	
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		28 OF 86	

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

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B

## Thunderbolt Connector A



B

A

8	7	6	5	4	3	2	1
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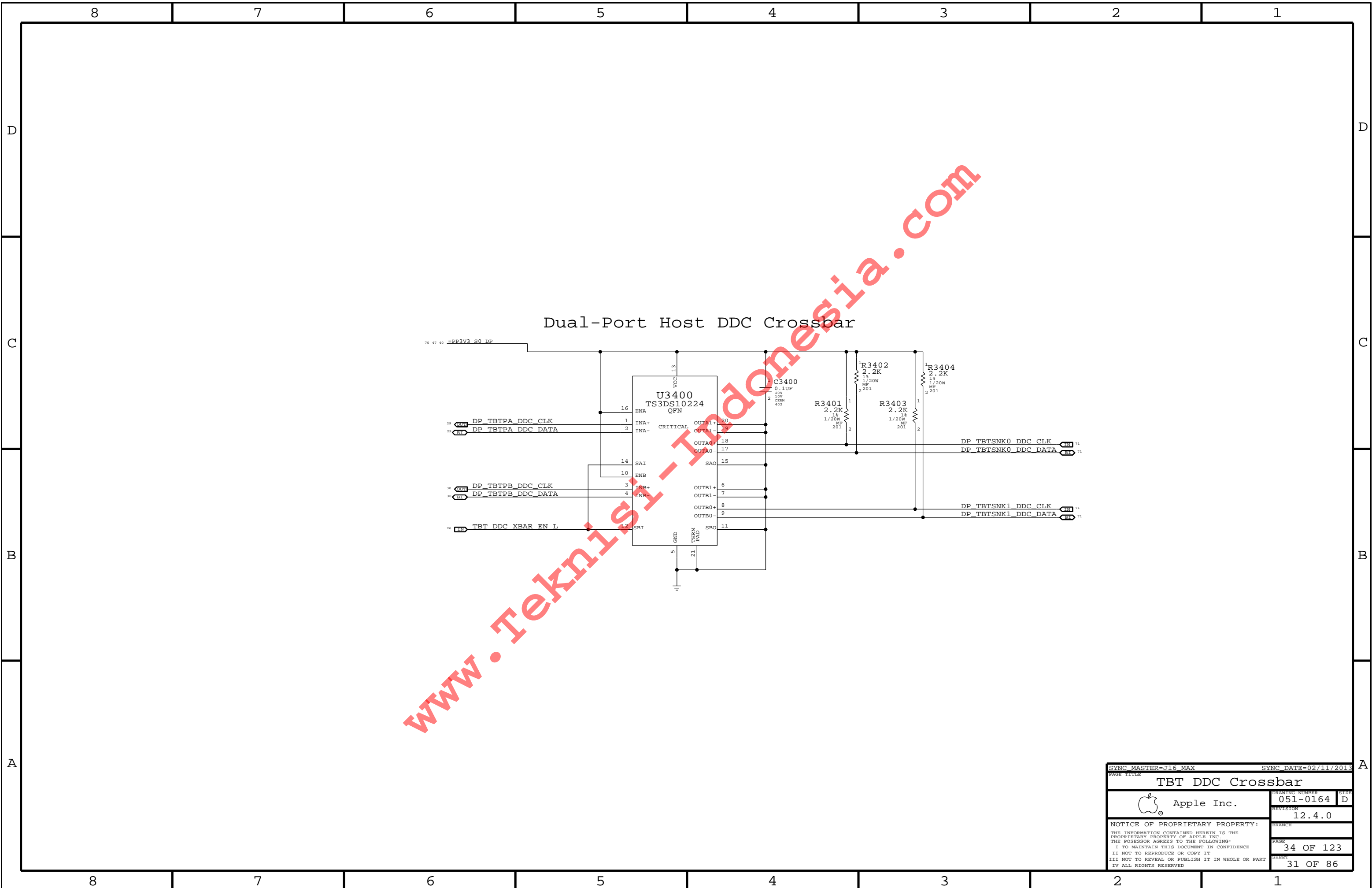
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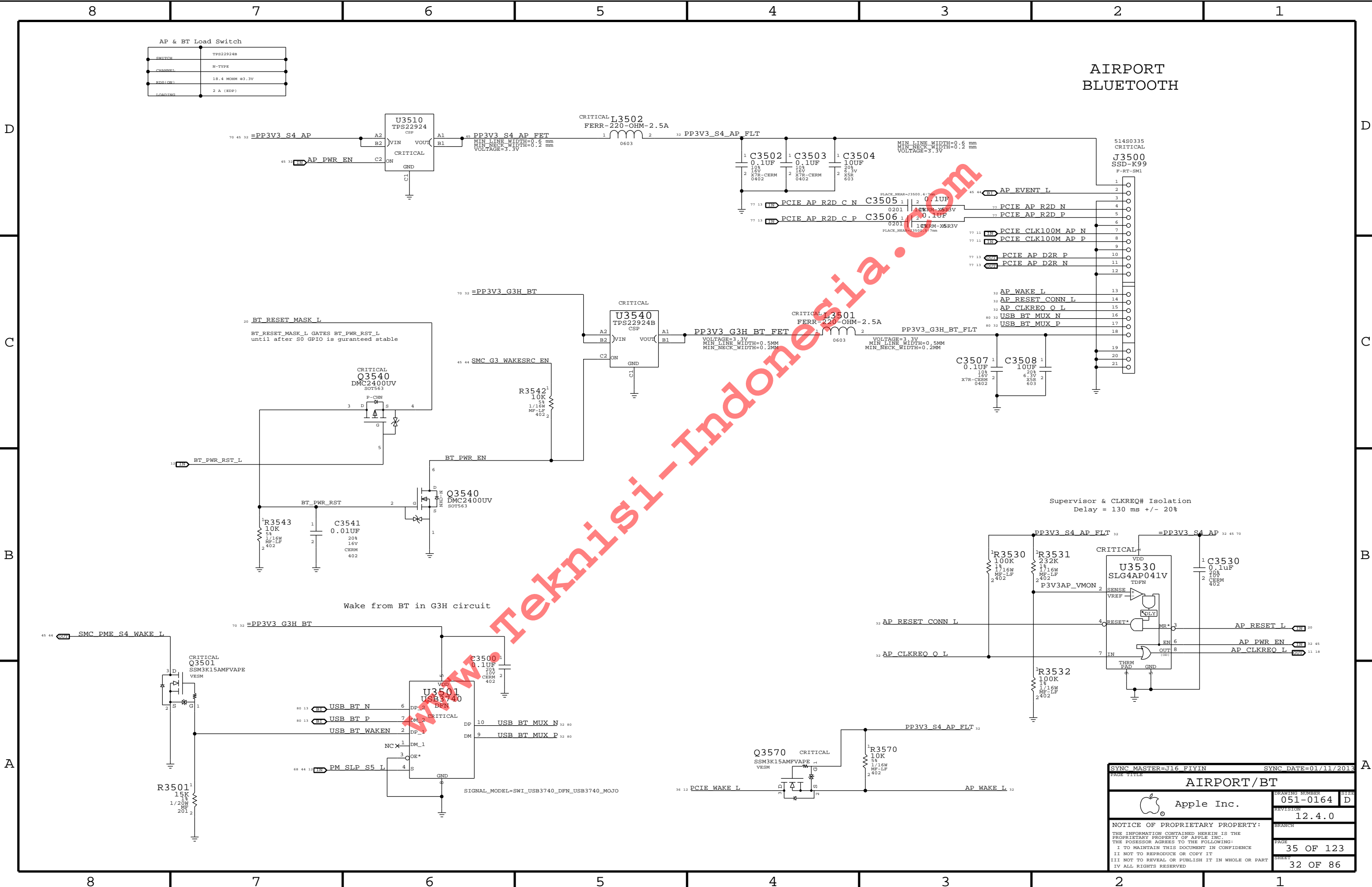


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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

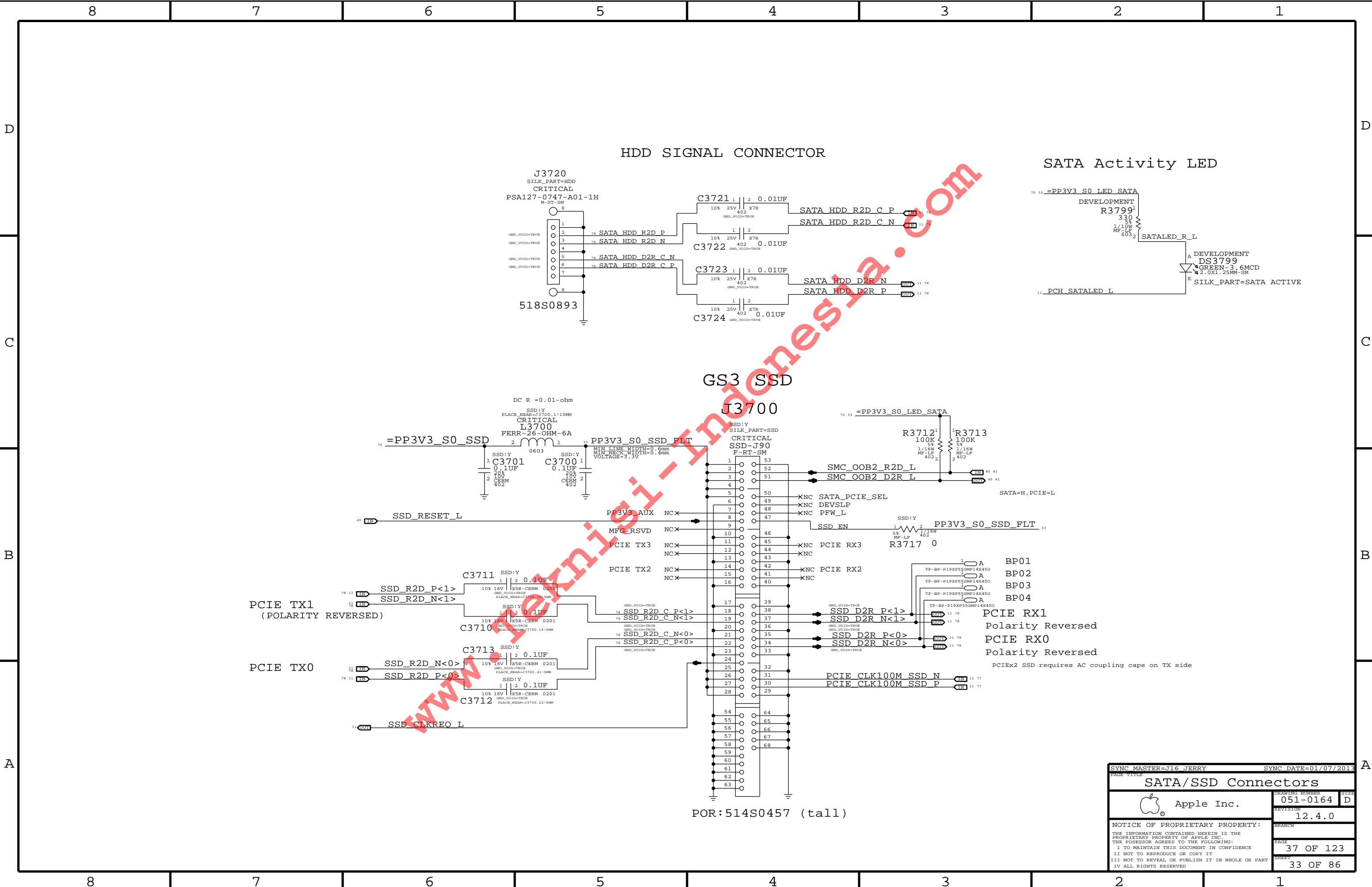





AP & BT Load Switch	
SWITCH	TPS22924B
CHANNEL	N-TYPE
RES(ON)	18.4 MOHM @3.3V
LOADING	2 A (RDP)

AIRPORT  
BLUETOOTH

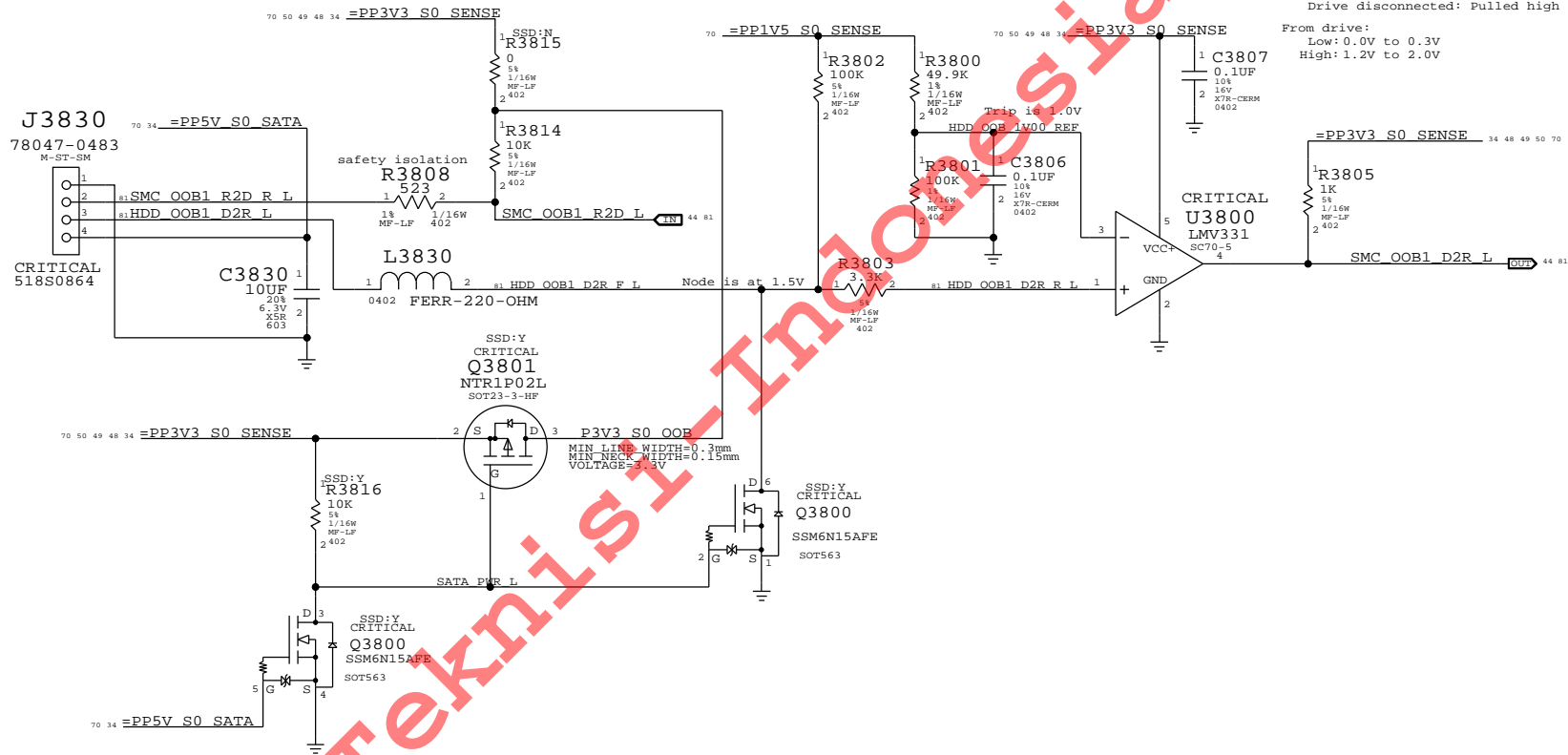
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AIRPORT/BT		DRAWING NUMBER	
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SATA/SSD Connectors			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE
	REVISION	12.4.0	D
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# HDD POWER/OOB CONNECTOR

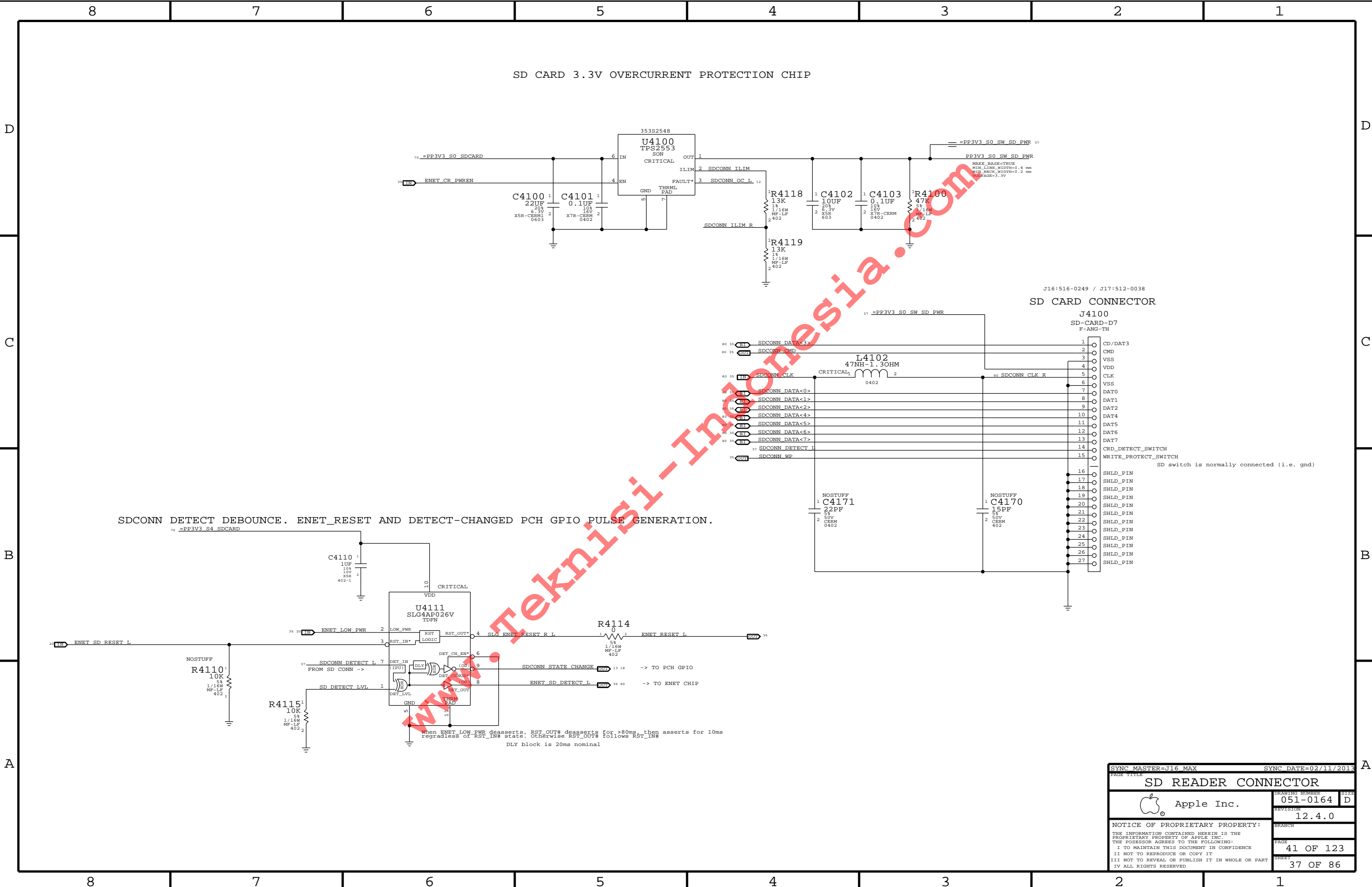
## HDD Out-of-Band Temperature Sensing



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HDD Connector			
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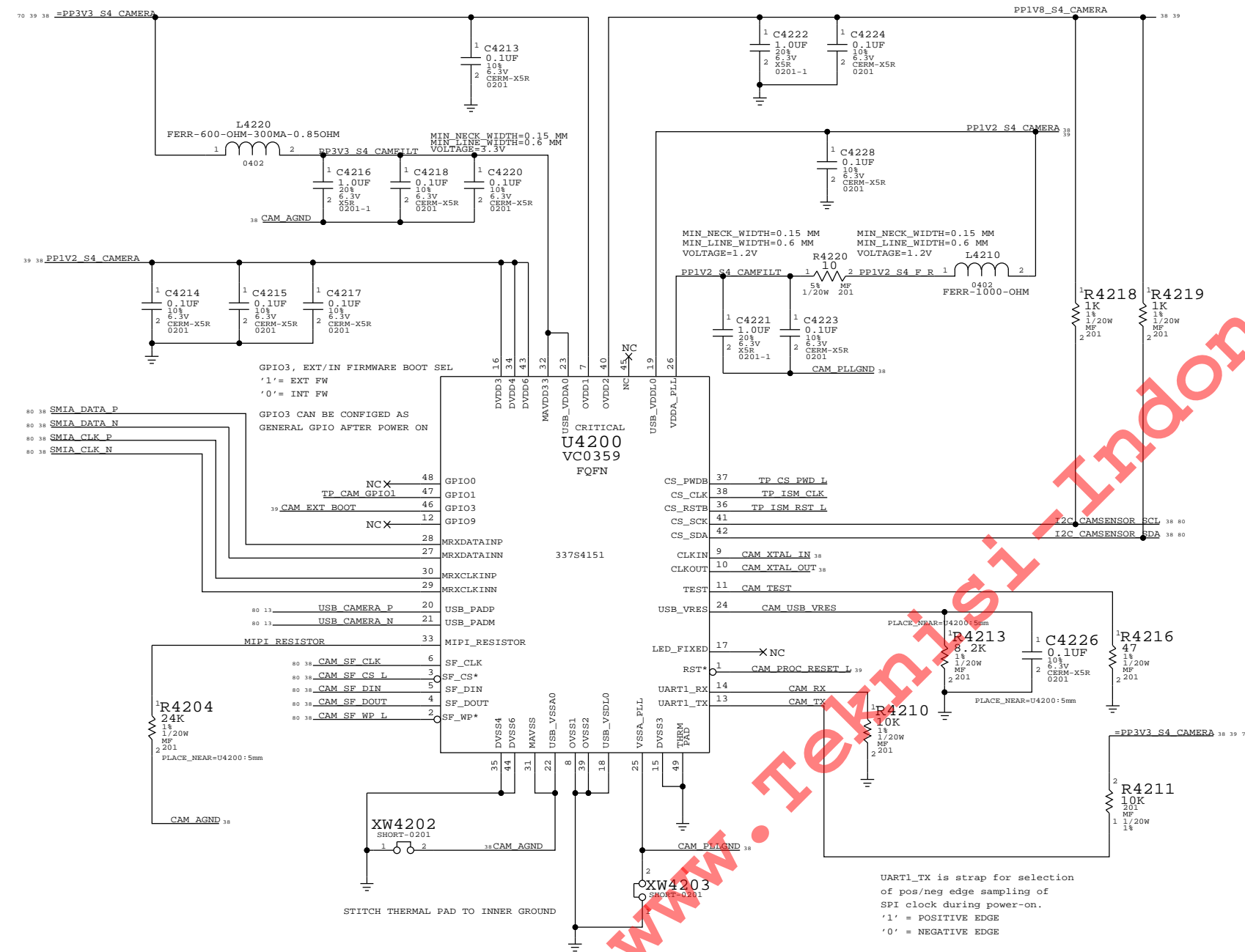
SDCONN DETECT DEBOUNCE. ENET\_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

When ENET LOW\_PWR deasserts, RST\_OUT# deasserts for >80ms, then asserts for 10ms regardless of RST\_IN# state. Otherwise RST\_OUT# follows RST\_IN#

DLY block is 20ms nominal

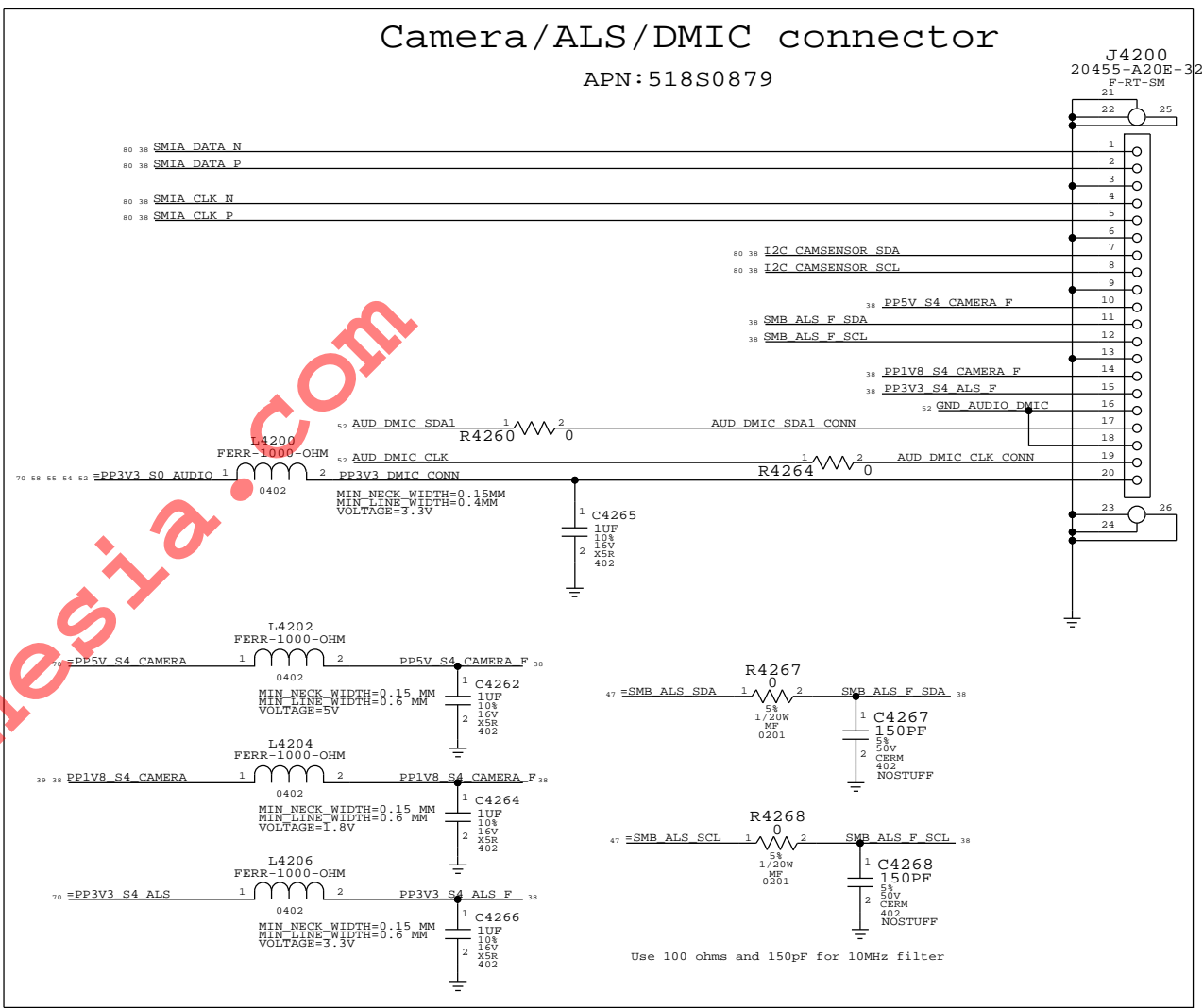
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SD READER CONNECTOR		41 OF 123	
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# USB CAMERA CONTROLLER

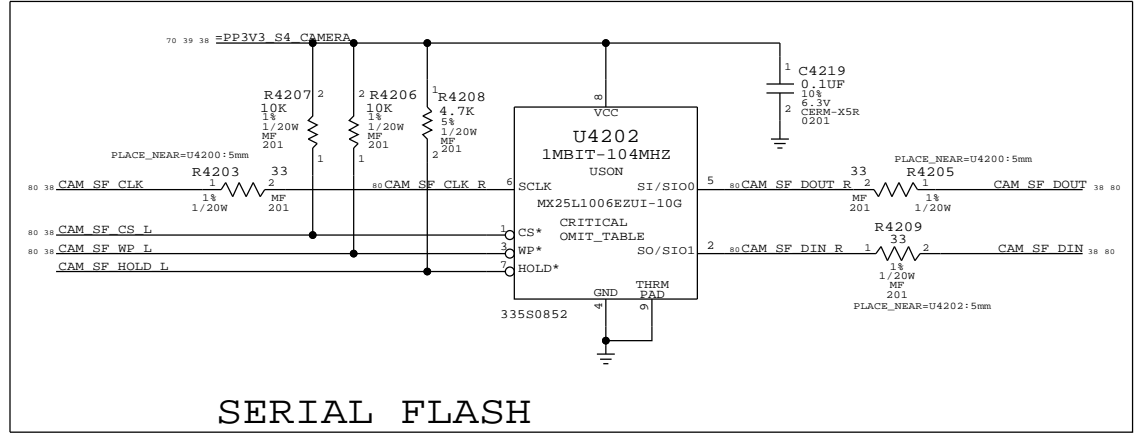


## Camera/ALS/DMIC connector

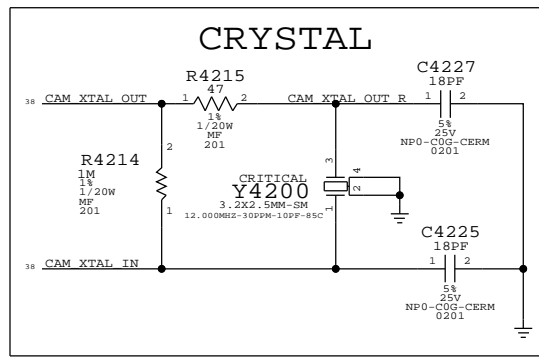
APN:518S0879



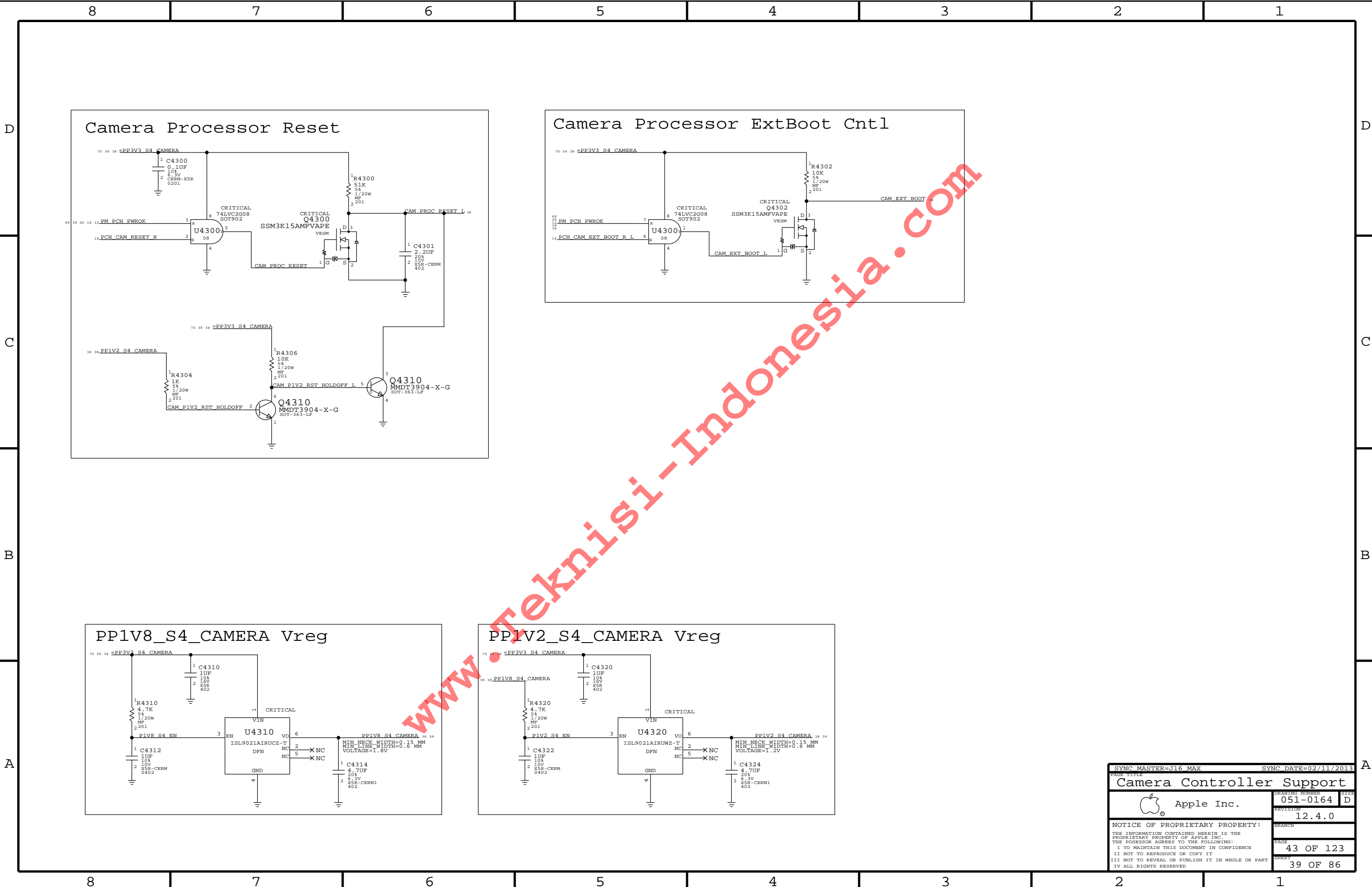
## SERIAL FLASH



## CRYSTAL



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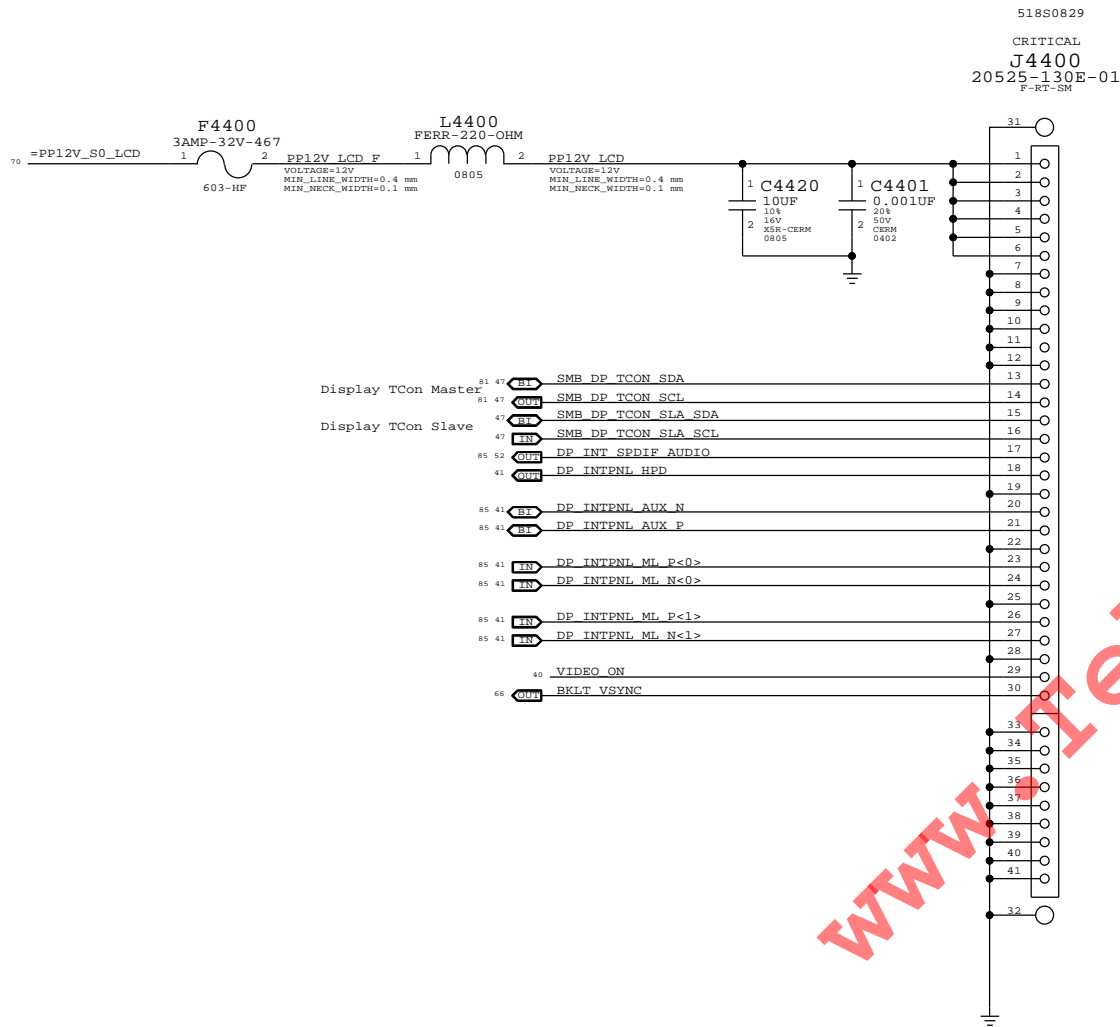
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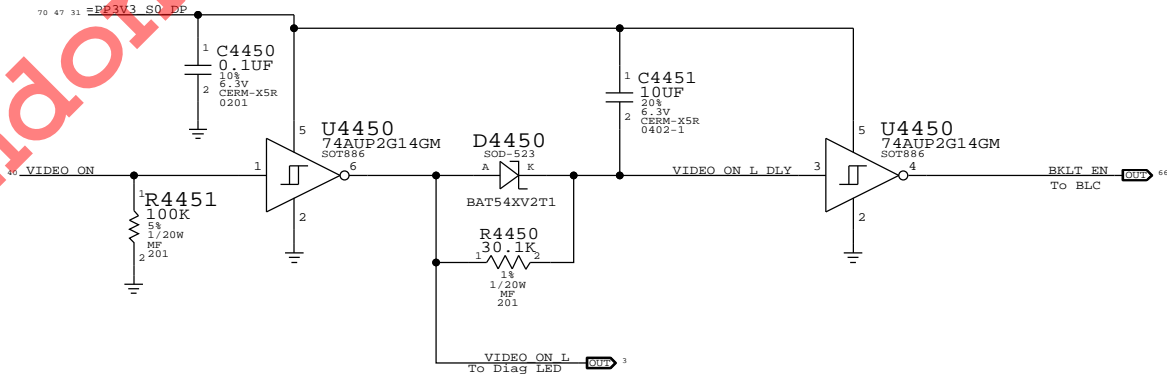
A


Internal DP Connector

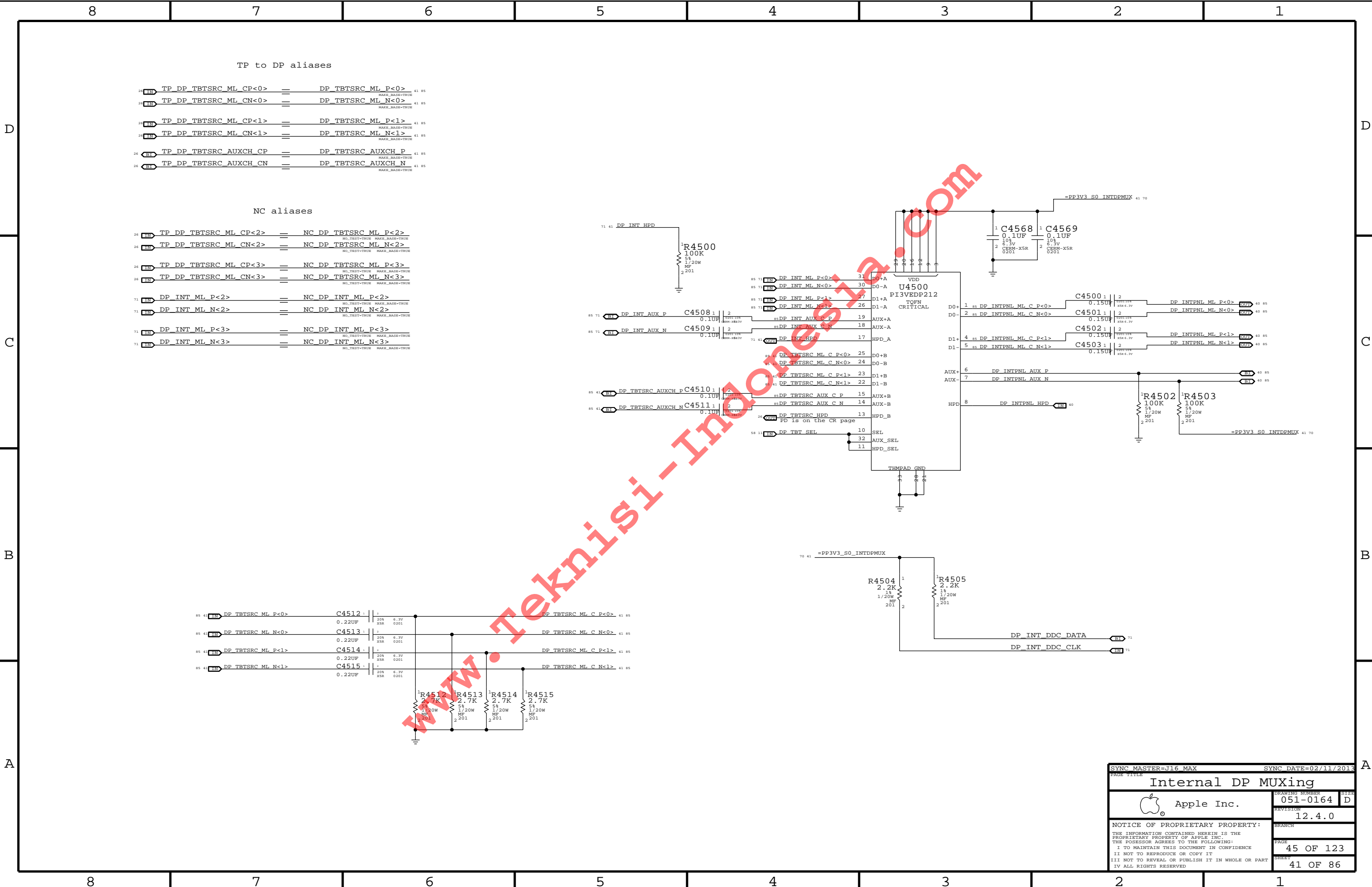


Backlight Control

Delay applies only on a L->H transition on VIDEO\_ON. This guarantees video is valid before the backlight is enabled.  
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video



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Internal DP Support			
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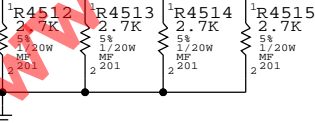
TP to DP aliases

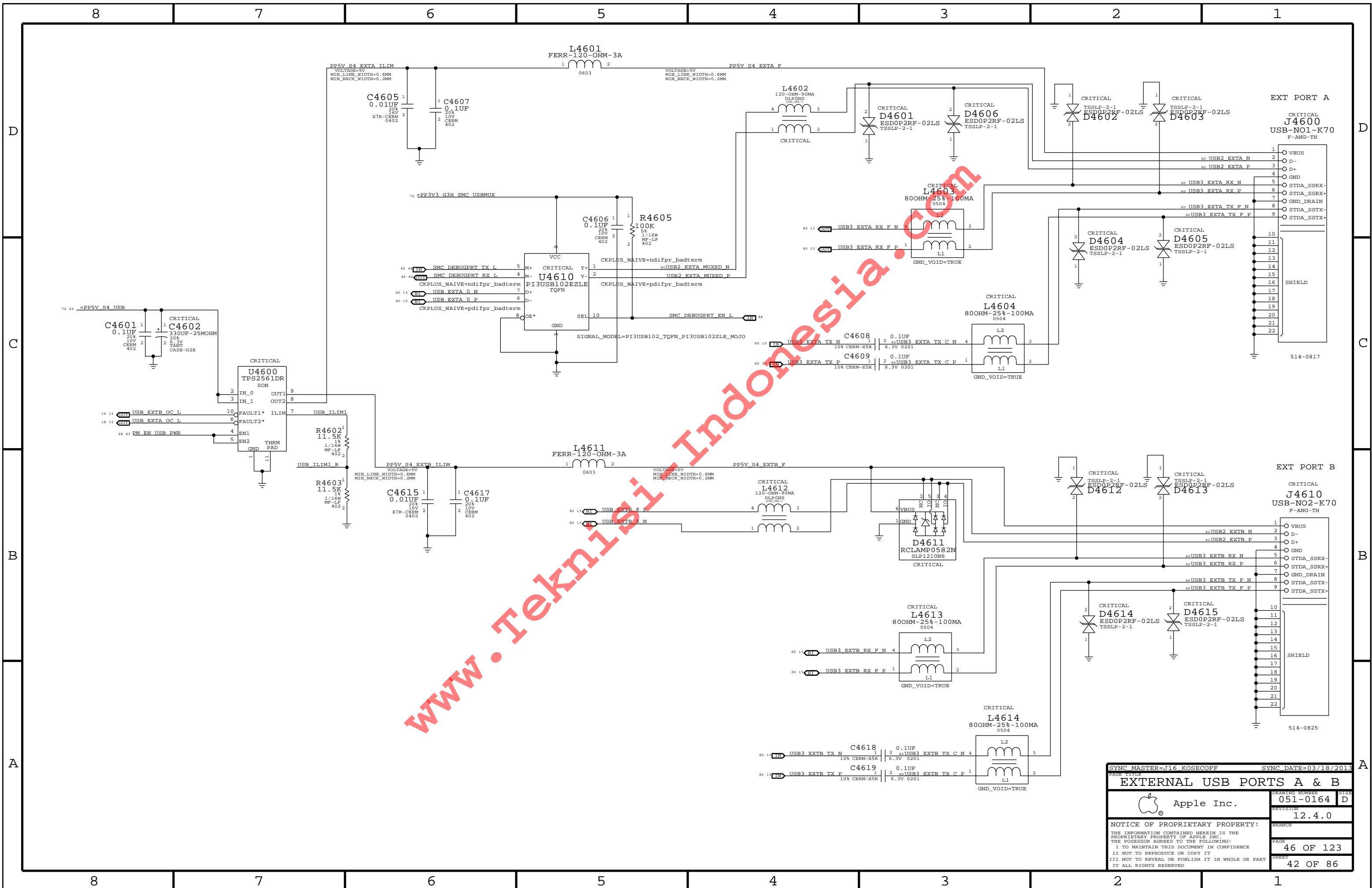
26	TP_DP_TBTSRC_ML_CP<0>	==	DP_TBTSRC_ML_P<0>	41 85
26	TP_DP_TBTSRC_ML_CN<0>	==	DP_TBTSRC_ML_N<0>	41 85
26	TP_DP_TBTSRC_ML_CP<1>	==	DP_TBTSRC_ML_P<1>	41 85
26	TP_DP_TBTSRC_ML_CN<1>	==	DP_TBTSRC_ML_N<1>	41 85
26	TP_DP_TBTSRC_AUXCH_CP	==	DP_TBTSRC_AUXCH_P	41 85
26	TP_DP_TBTSRC_AUXCH_CN	==	DP_TBTSRC_AUXCH_N	41 85


NC aliases

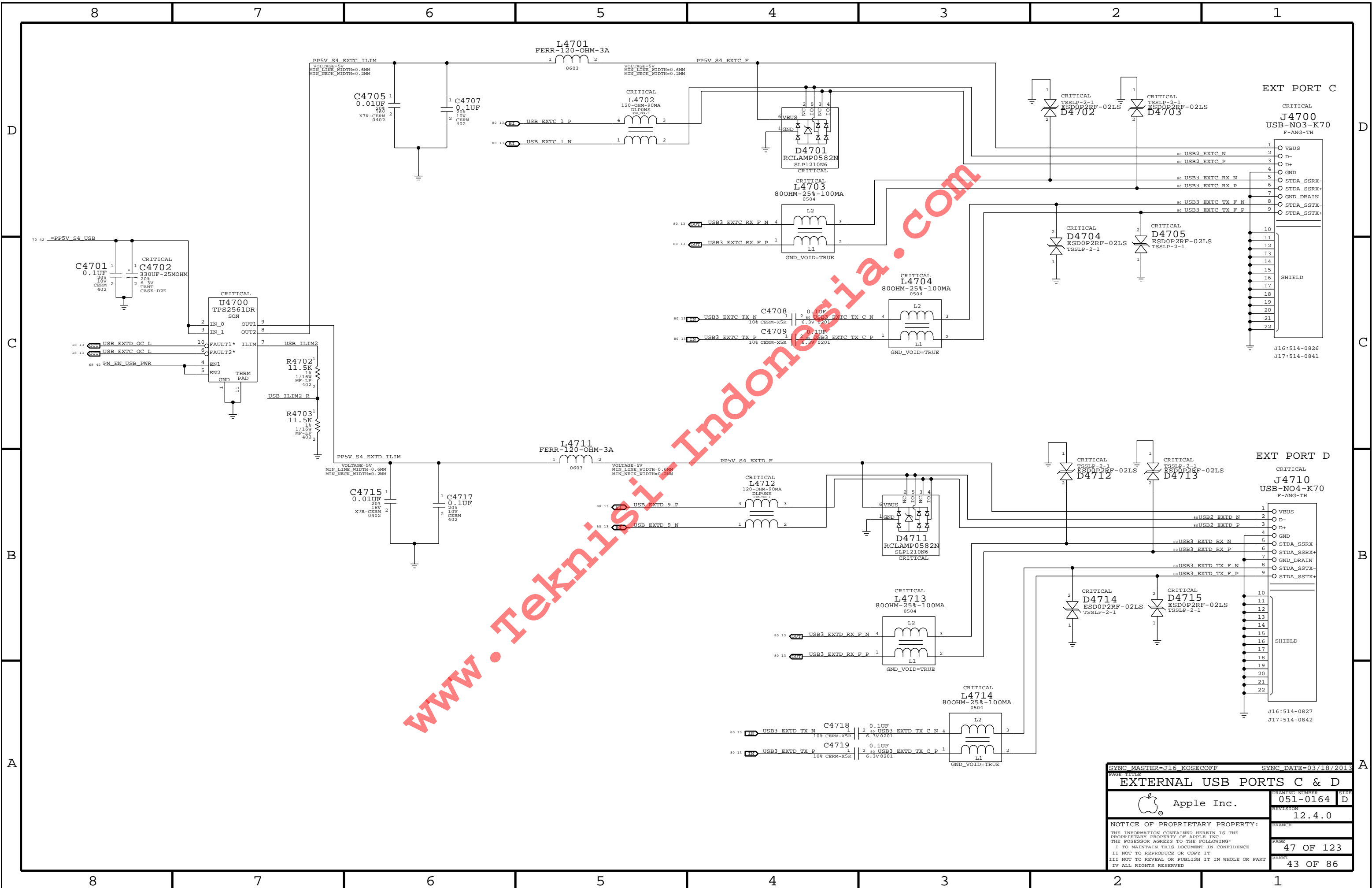
26	TP_DP_TBTSRC_ML_CP<2>	==	NC_DP_TBTSRC_ML_P<2>	41 85
26	TP_DP_TBTSRC_ML_CN<2>	==	NC_DP_TBTSRC_ML_N<2>	41 85
26	TP_DP_TBTSRC_ML_CP<3>	==	NC_DP_TBTSRC_ML_P<3>	41 85
26	TP_DP_TBTSRC_ML_CN<3>	==	NC_DP_TBTSRC_ML_N<3>	41 85
71	DP_INT_ML_P<2>	==	NC_DP_INT_ML_P<2>	41 85
71	DP_INT_ML_N<2>	==	NC_DP_INT_ML_N<2>	41 85
71	DP_INT_ML_P<3>	==	NC_DP_INT_ML_P<3>	41 85
71	DP_INT_ML_N<3>	==	NC_DP_INT_ML_N<3>	41 85


85 41	DP_TBTSRC_ML_P<0>	C4512	0.22UF	20% 6.3V XSR 0201	DP_TBTSRC_ML_C_P<0>	41 85
85 41	DP_TBTSRC_ML_N<0>	C4513	0.22UF	20% 6.3V XSR 0201	DP_TBTSRC_ML_C_N<0>	41 85
85 41	DP_TBTSRC_ML_P<1>	C4514	0.22UF	20% 6.3V XSR 0201	DP_TBTSRC_ML_C_P<1>	41 85
85 41	DP_TBTSRC_ML_N<1>	C4515	0.22UF	20% 6.3V XSR 0201	DP_TBTSRC_ML_C_N<1>	41 85

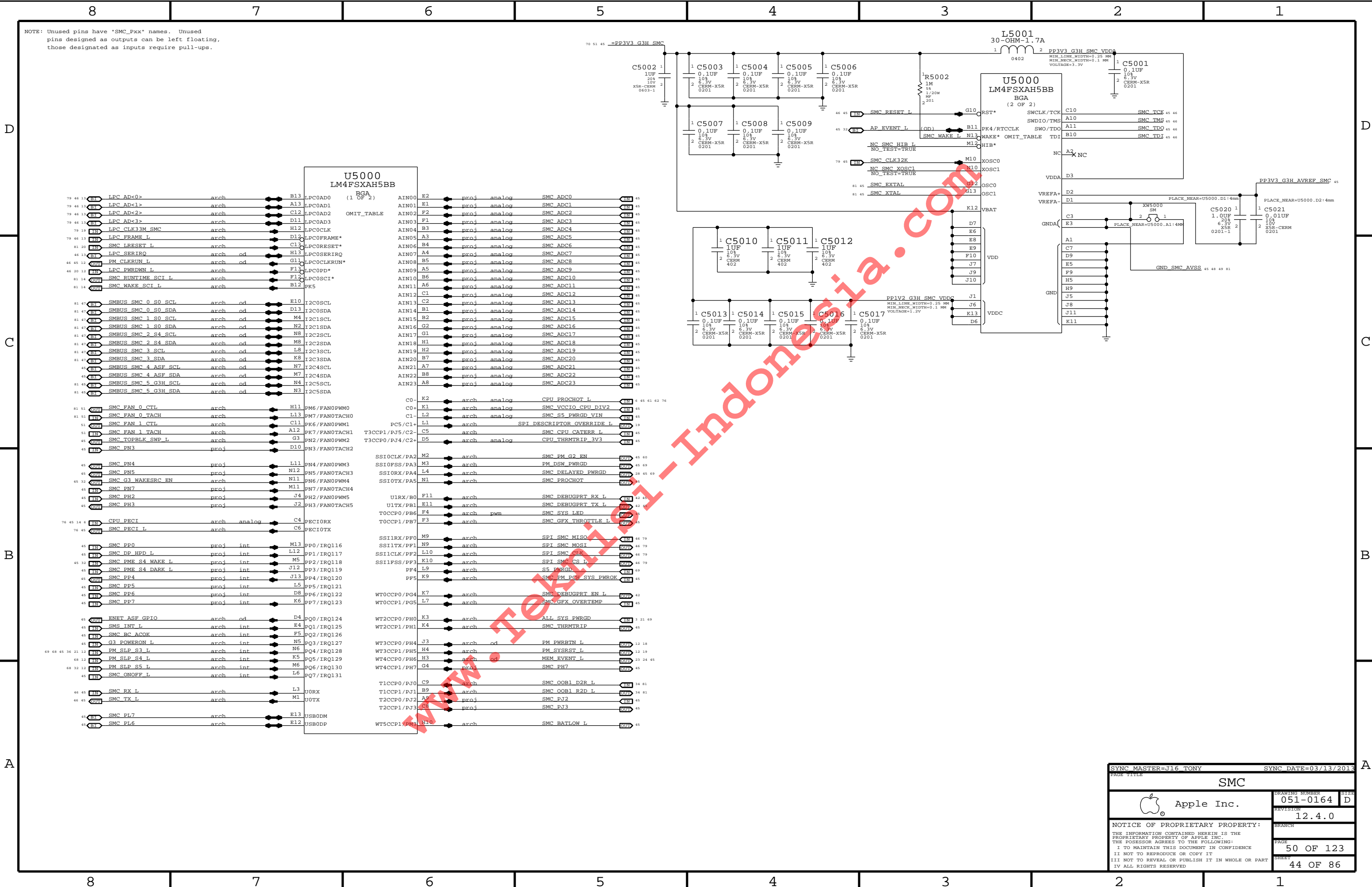


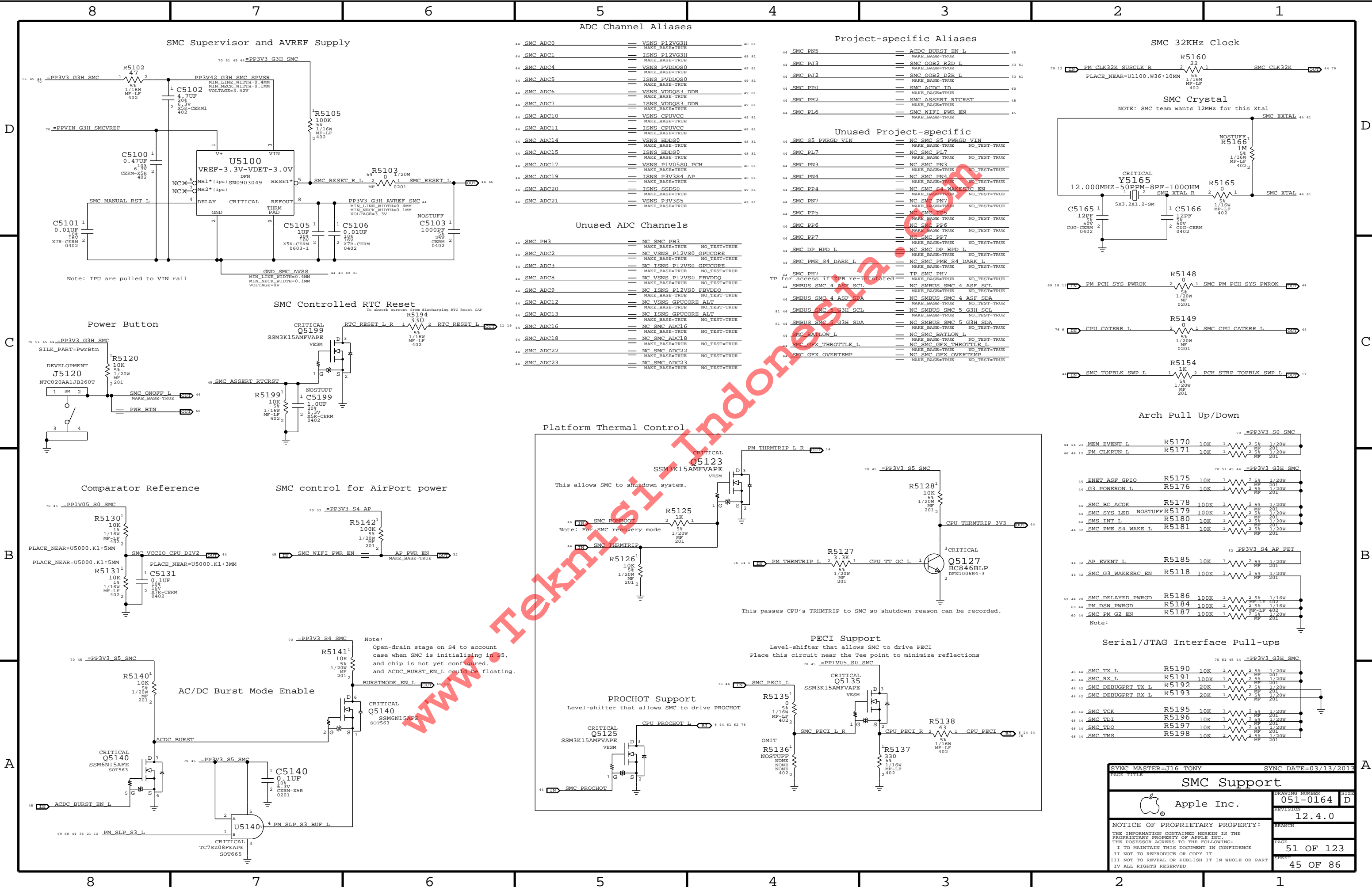


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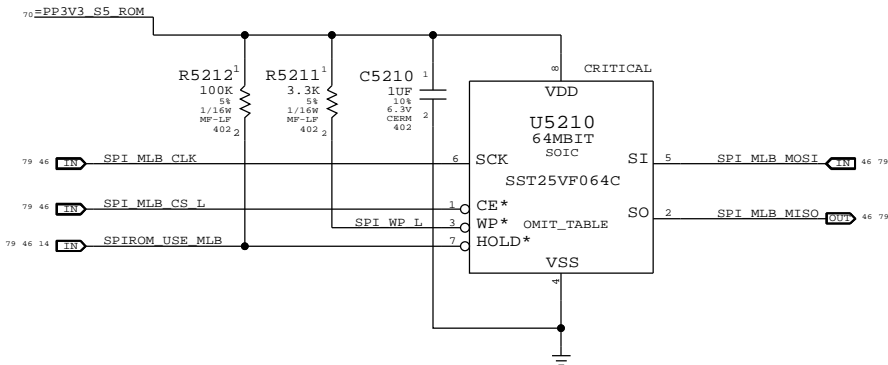
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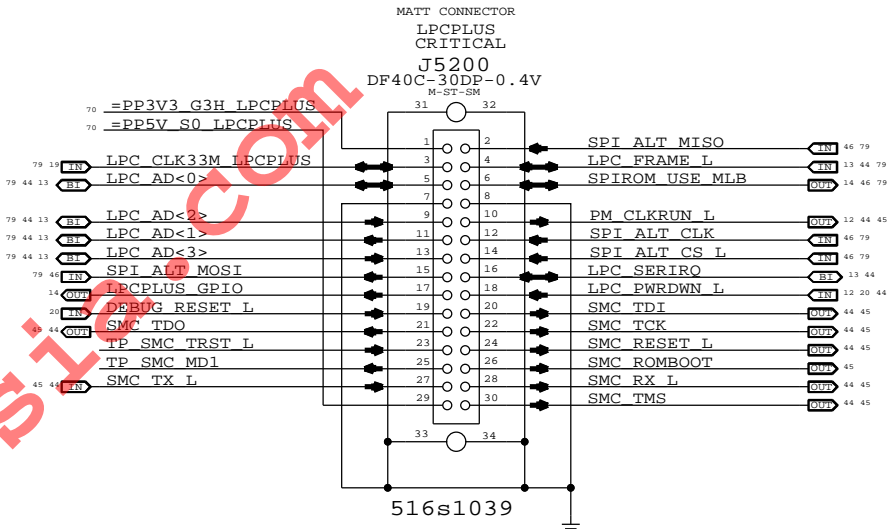
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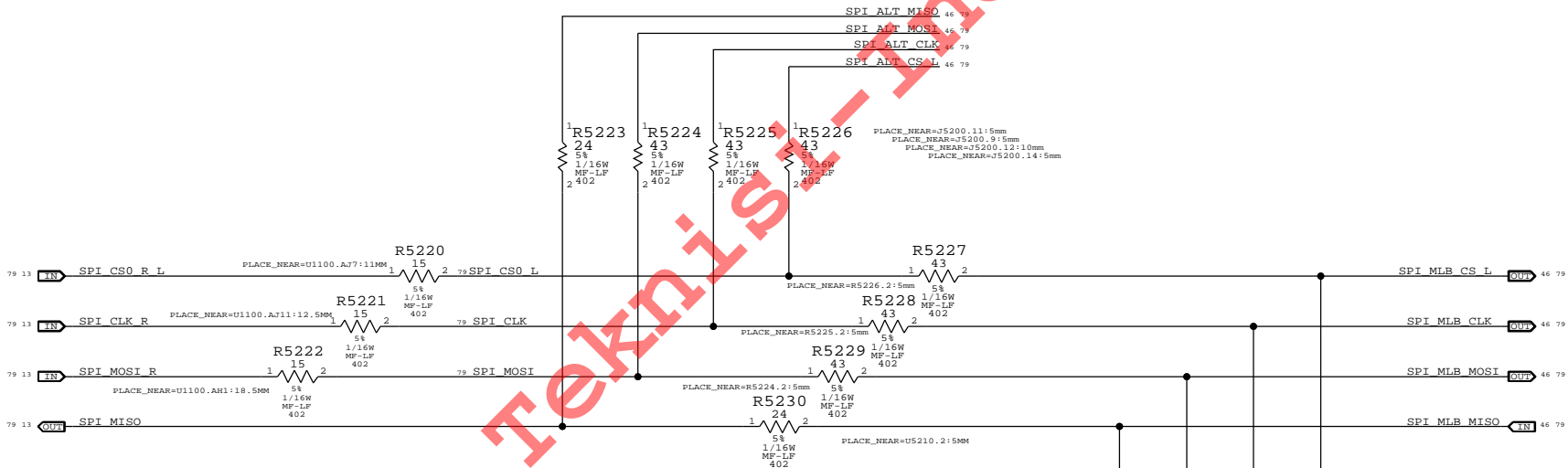
### SPI BootROM



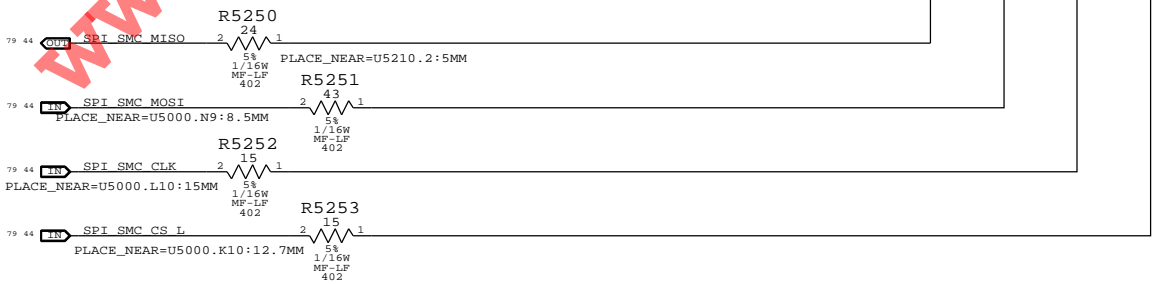
### LPC+SPI Connector




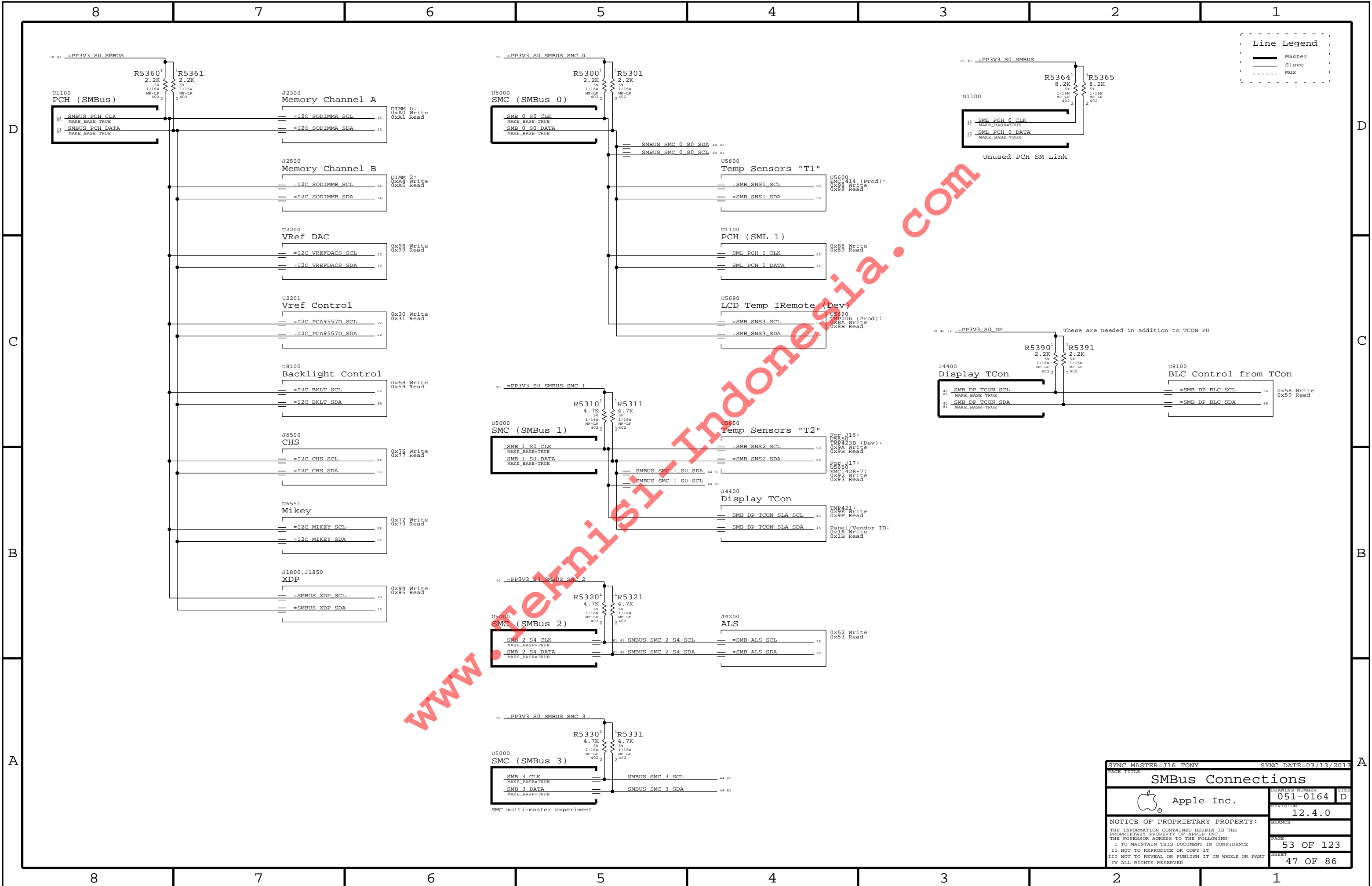
### SPI Series Termination

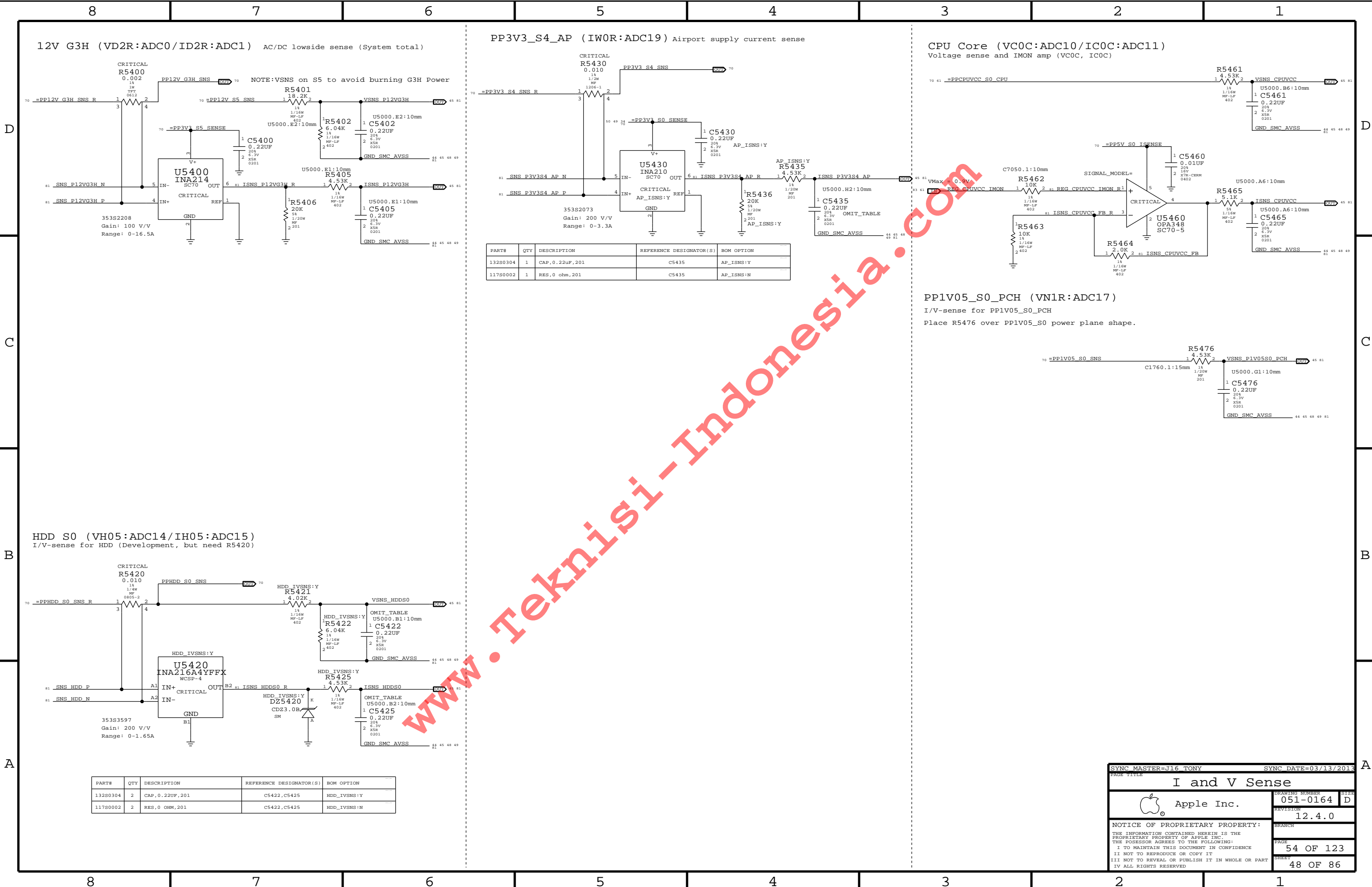


### SMC SPI Support

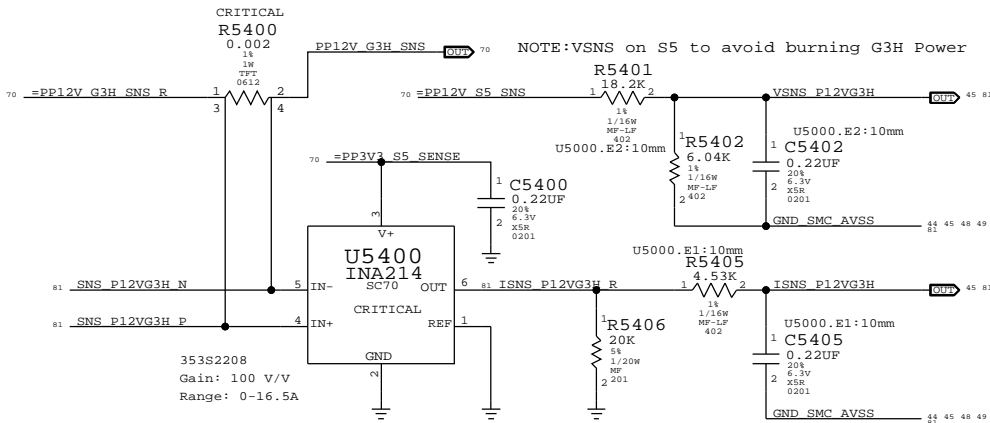


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SPI and Debug Connector			
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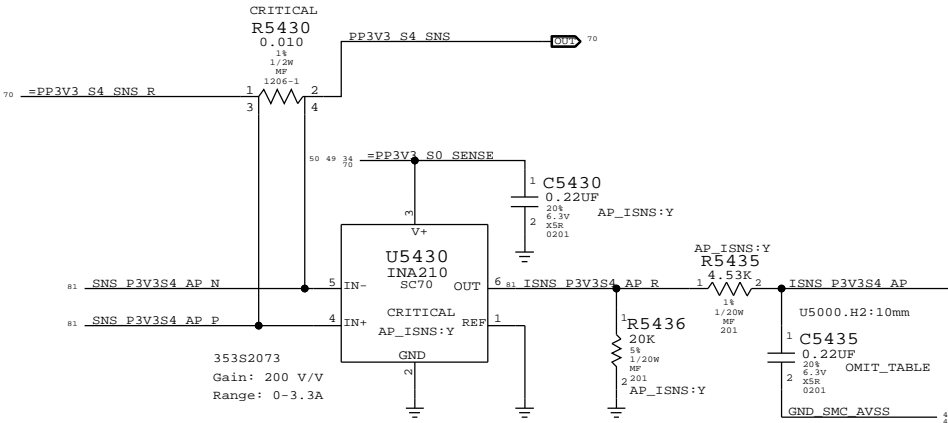




12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)

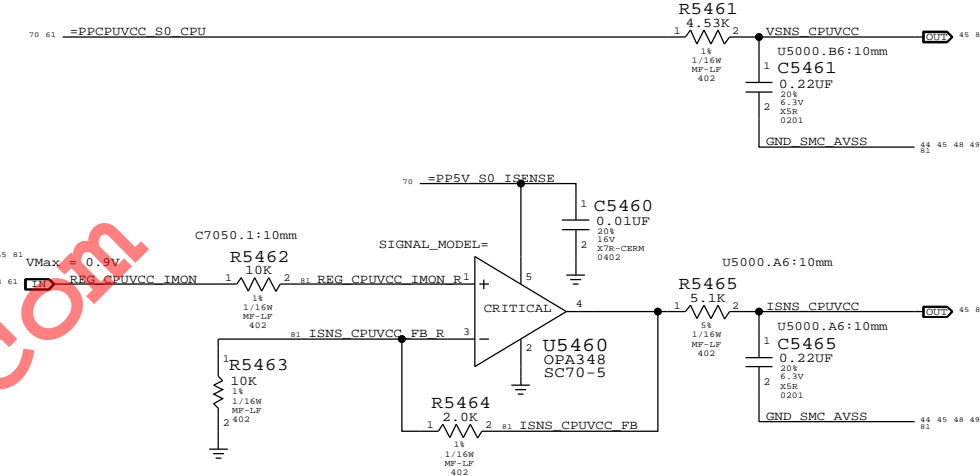


PP3V3\_S4\_AP (IW0R:ADC19) Airport supply current sense



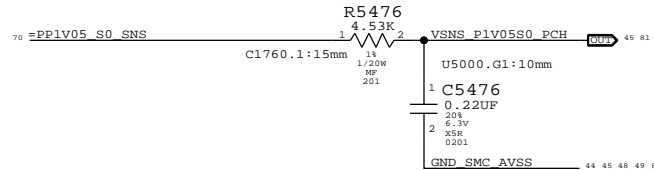
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22uF,201	C5435	AP_ISNS:Y
117S0002	1	RES,0 ohm,201	C5435	AP_ISNS:N

CPU Core (VC0C:ADC10/IC0C:ADC11)  
Voltage sense and IMON amp (VC0C, IC0C)

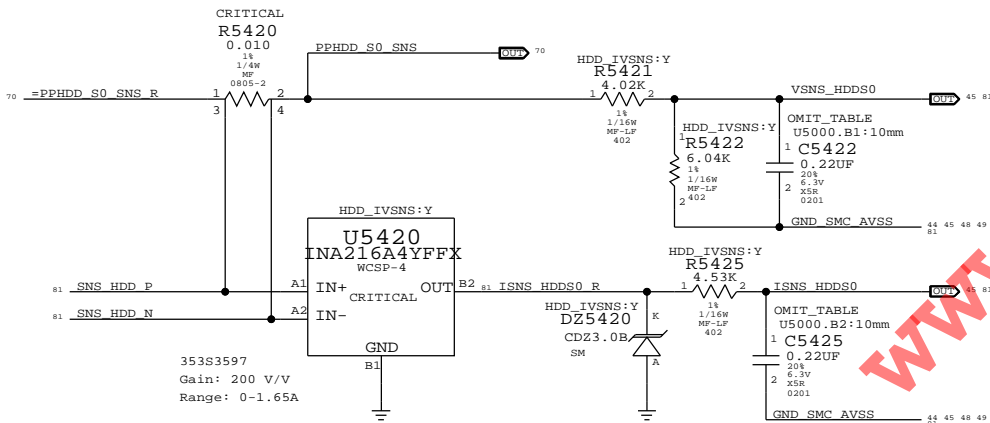


PP1V05\_S0\_PCH (VN1R:ADC17)

I/V-sense for PP1V05\_S0\_PCH  
Place R5476 over PP1V05\_S0 power plane shape.



HDD S0 (VH05:ADC14/IH05:ADC15)  
I/V-sense for HDD (Development, but need R5420)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22uF,201	C5422,C5425	HDD_IVSNS:Y
117S0002	2	RES,0 OHM,201	C5422,C5425	HDD_IVSNS:N

SYNC MASTER=J16 TONY

SYNC DATE=03/13/2013

I and V Sense

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12.4.0

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D

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A

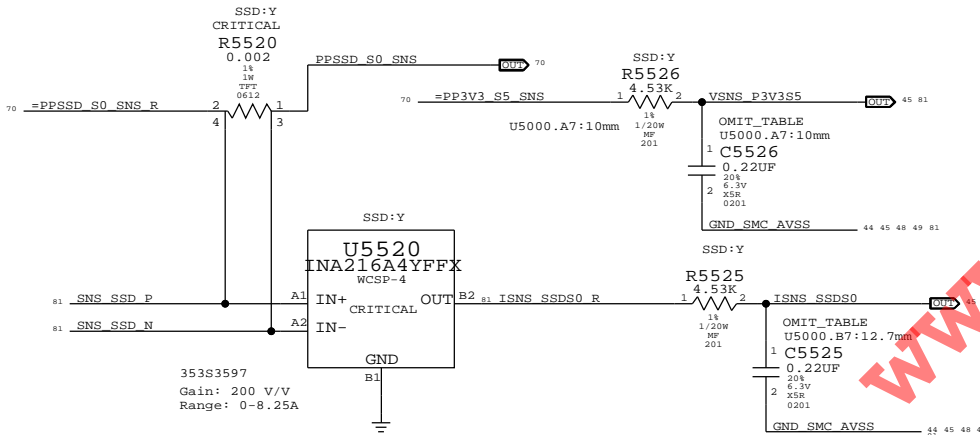
D

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B

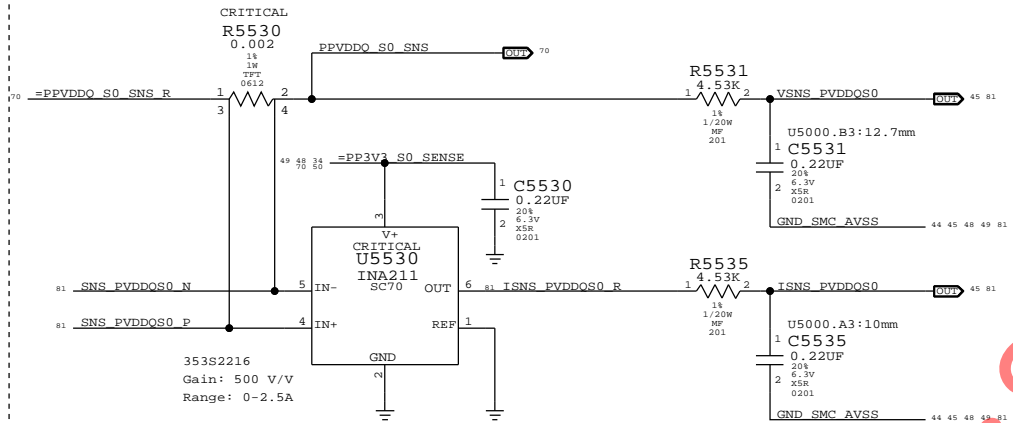
A

SSD S0 (IH1R:ADC20/VR3R:ADC21) I-sense for SSD / V-sense for PP3V3\_S5)

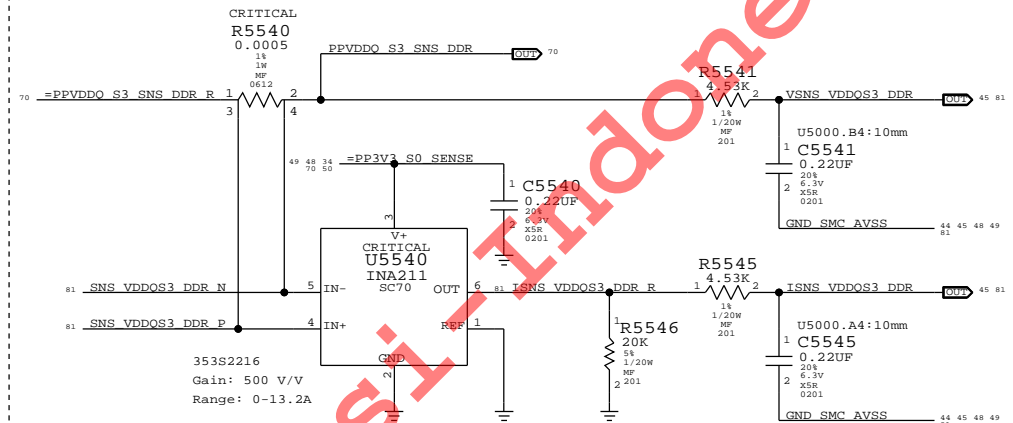



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0002	2	RES,0 OHM,201	C5525,C5526	SSD:N

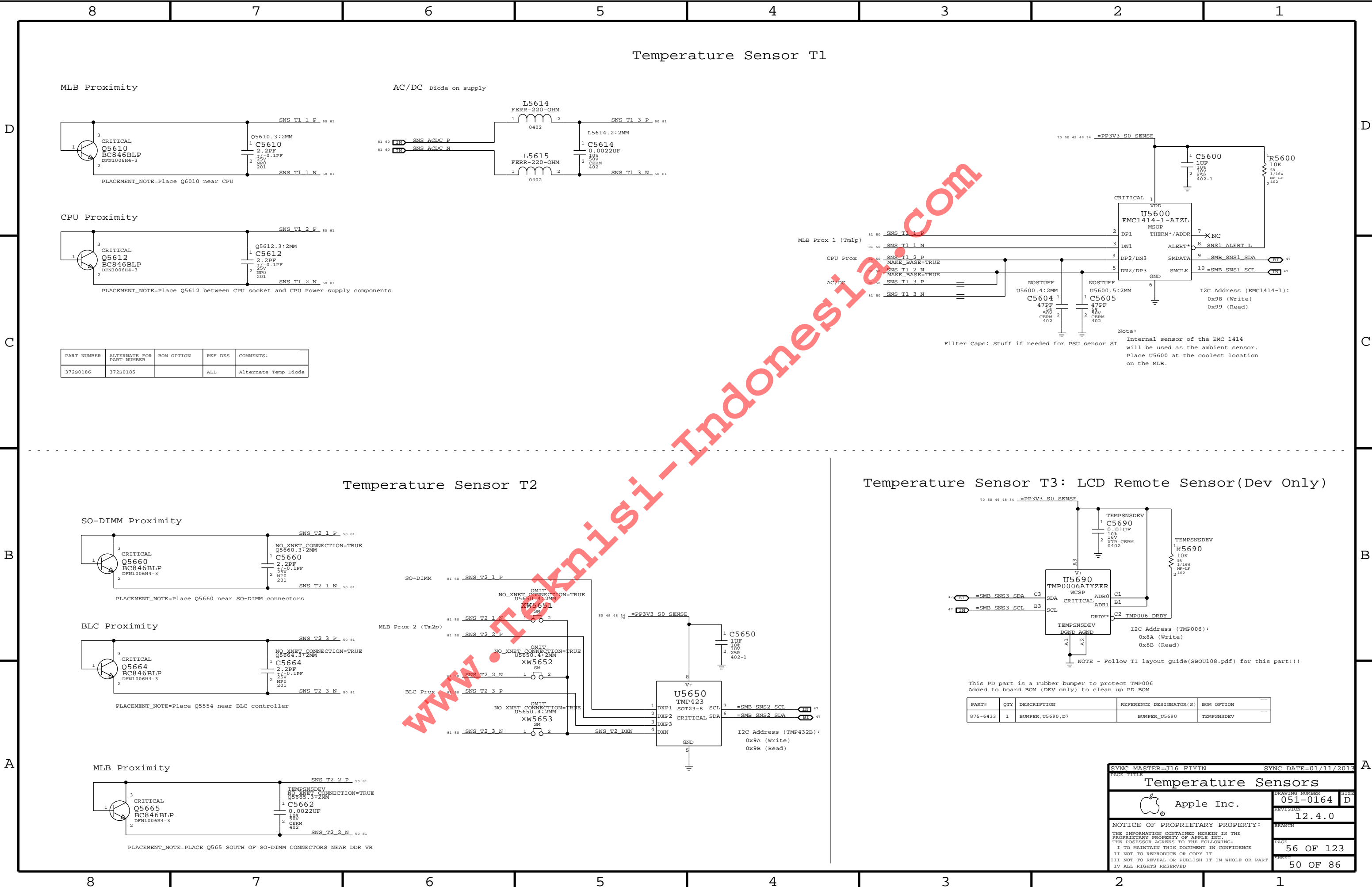
PPVDDQ\_S0 (VC0M:ADC4/IC0M:ADC5)  
lowside sense for CPU mem rail (2.5A max draw, 3.3A max sense capability)



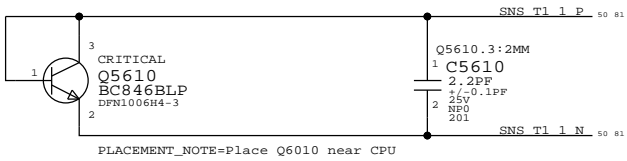
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)  
VDDQ lowside sense for SO-DIMM modules



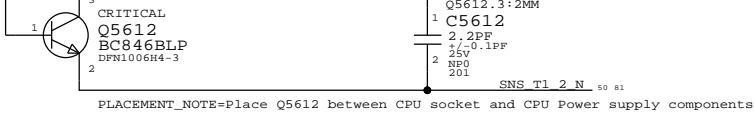
SYNC MASTER=J16 TONY		SYNC DATE=03/13/2013	
PAGE TITLE			
I and V Sense(Continued)			
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		SIZE	D
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MLB Proximity

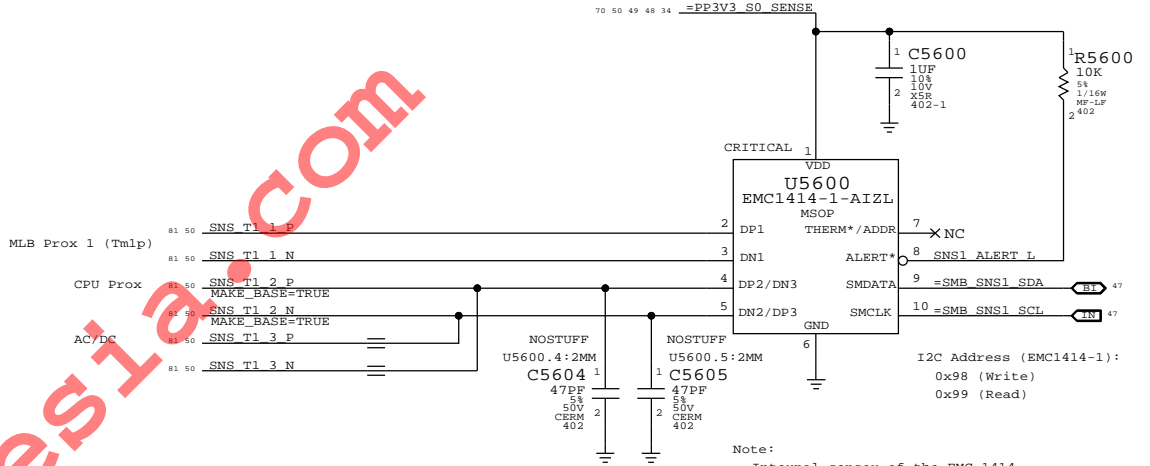
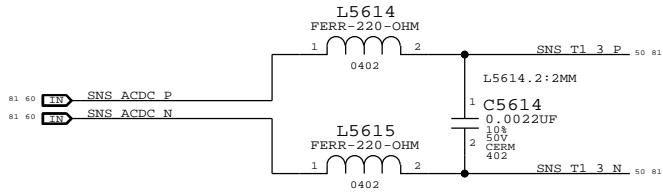


CPU Proximity



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

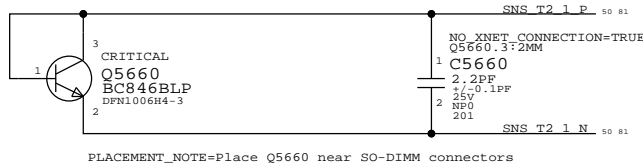
AC/DC Diode on supply



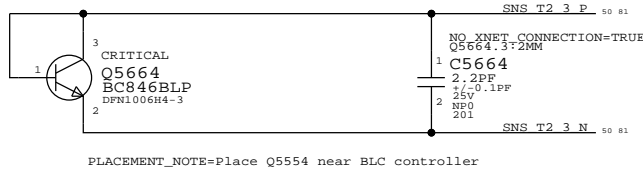
Note:  
Internal sensor of the EMC 1414 will be used as the ambient sensor. Place U5600 at the coolest location on the MLB.

Temperature Sensor T2

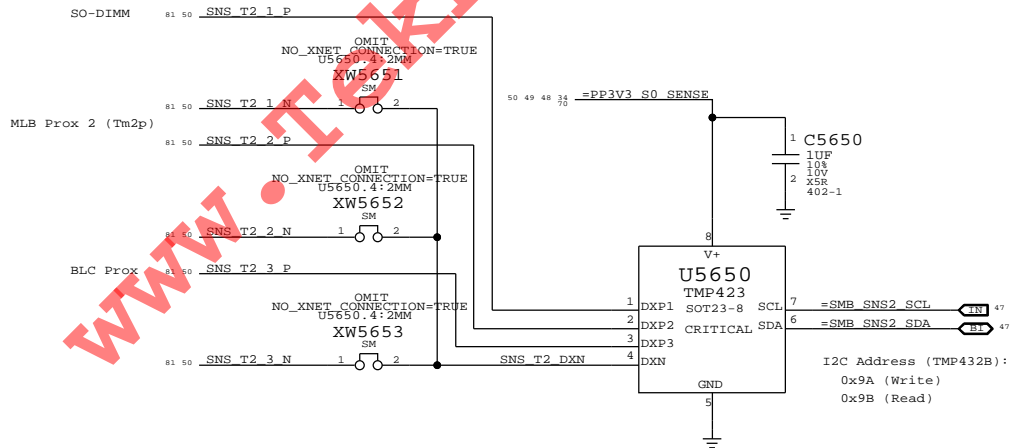
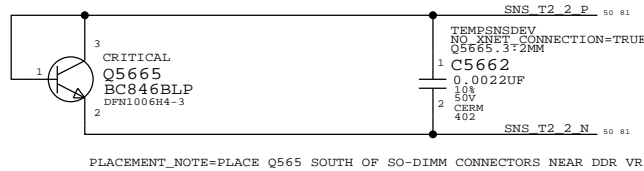
SO-DIMM Proximity



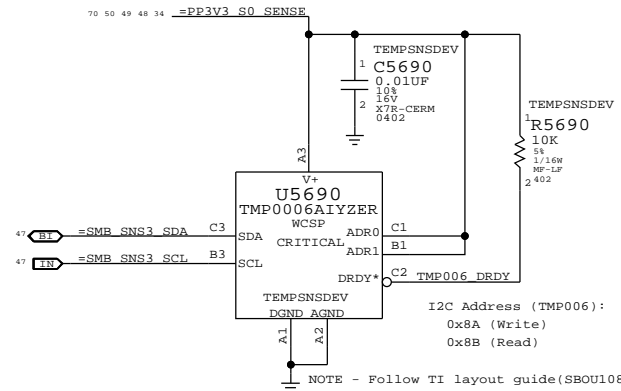
BLC Proximity



MLB Proximity




Temperature Sensor T3: LCD Remote Sensor (Dev Only)



This PD part is a rubber bumper to protect TMP006 Added to board BOM (DEV only) to clean up PD BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
875-6433	1	BUMPER,U5690,D7	BUMPER_U5690	TEMPSNSDEV

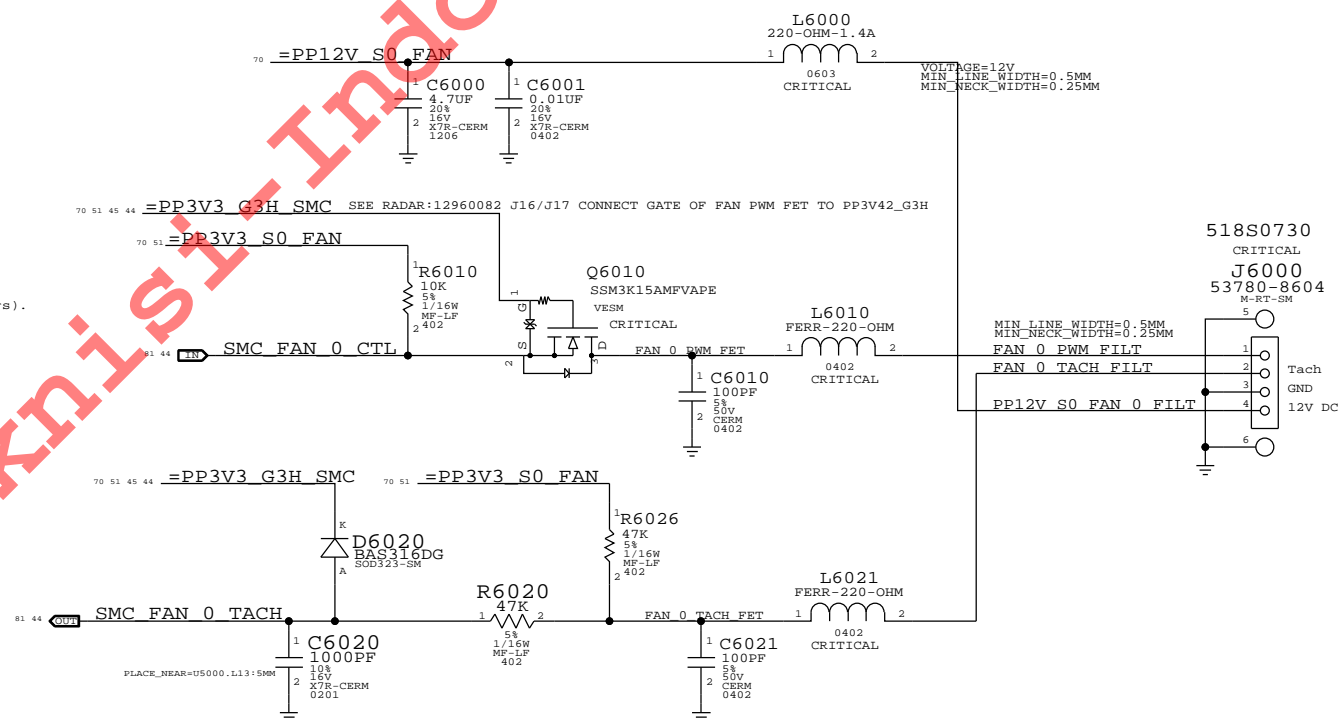
SYNC MASTER=J16 FIYIN		SYNC DATE=01/11/2013	
PAGE TITLE			
Temperature Sensors			
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		PAGE	
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Note:

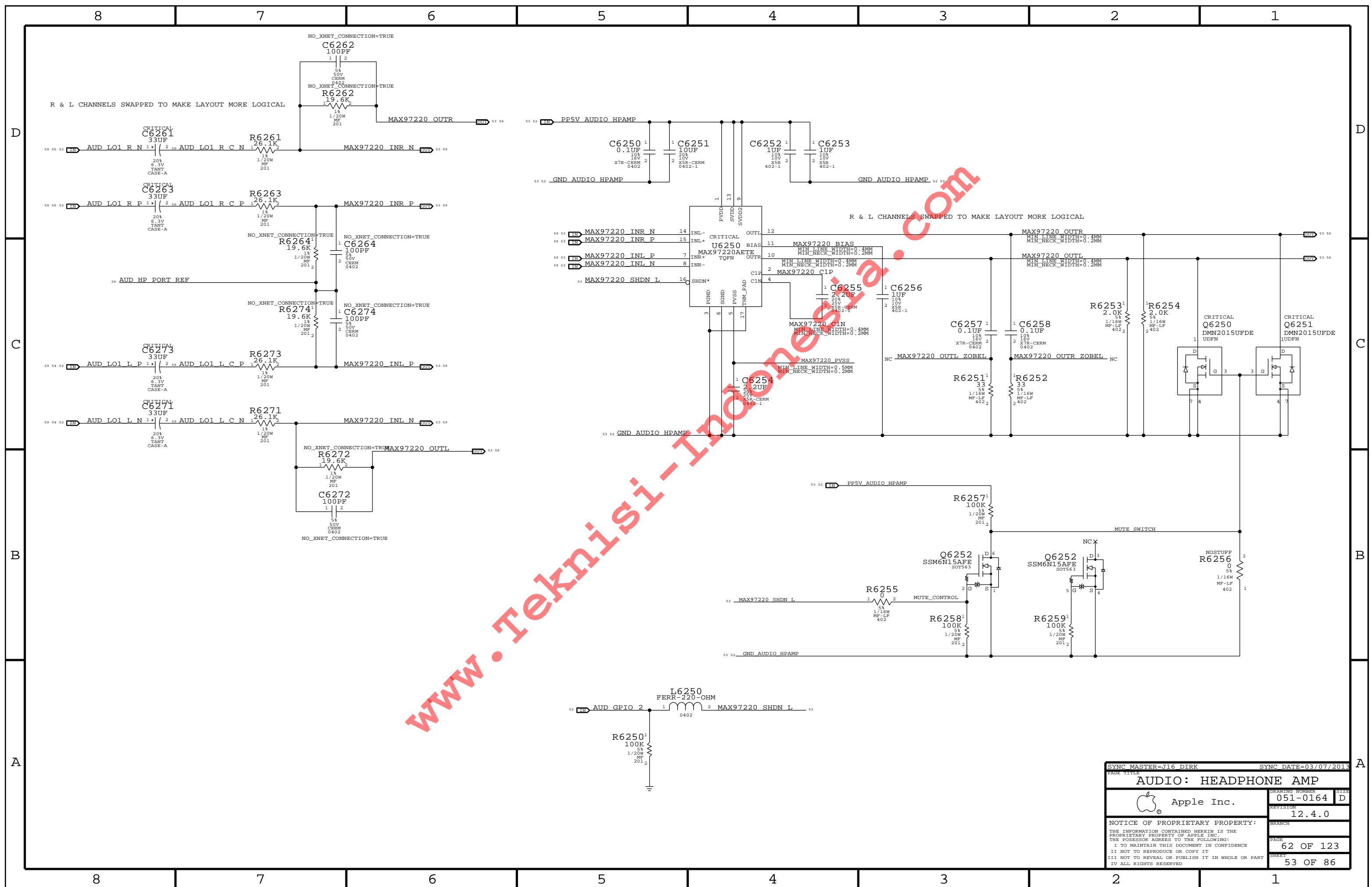
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

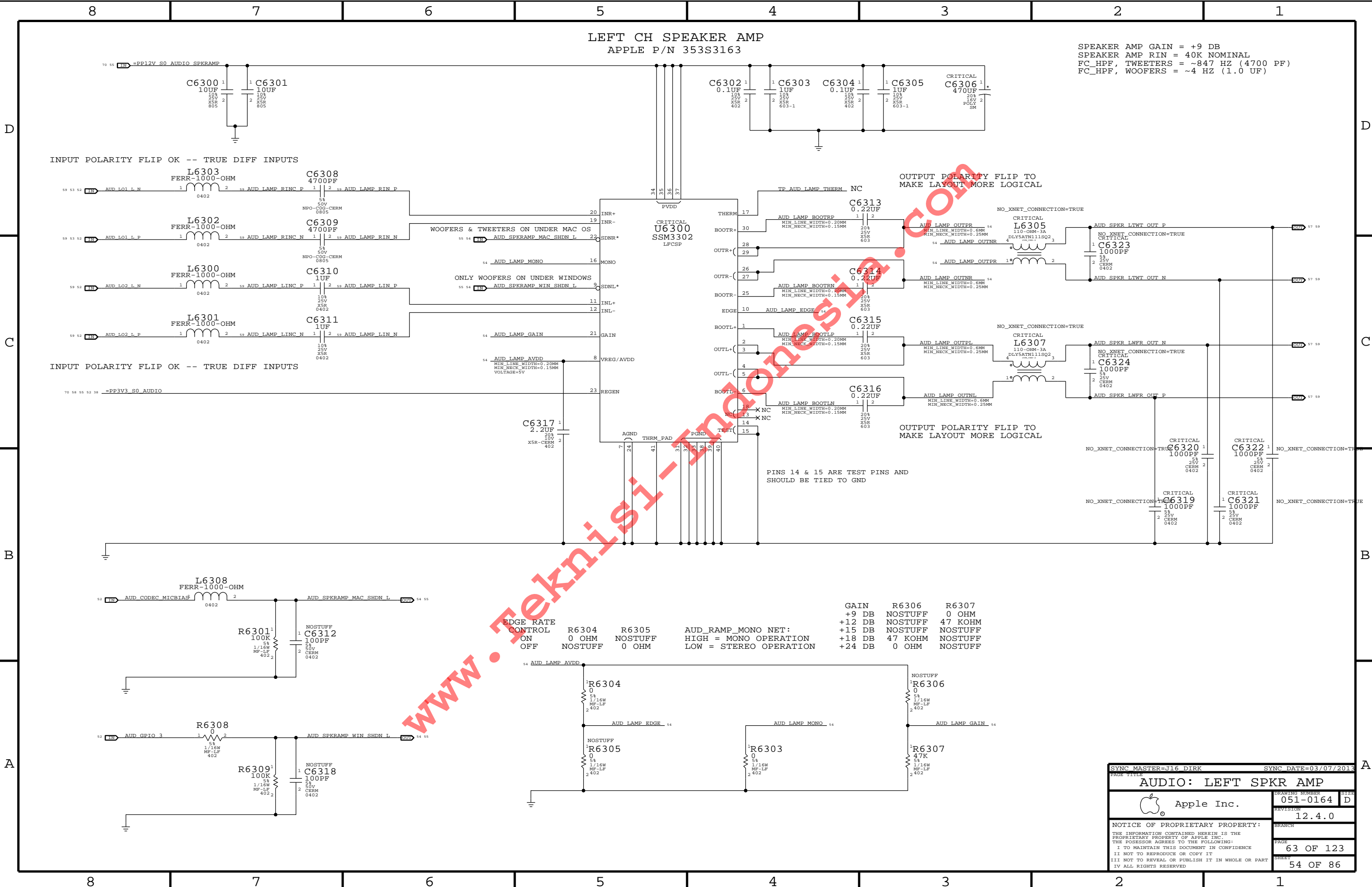
This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.  
See RADAR: 10565825- D7: Need schematic and PCB file of fan(All Vendors).









SPEAKER AMP GAIN = +9 DB  
SPEAKER AMP RIN = 40K NOMINAL  
FC\_HPF, TWEETERS = ~847 HZ (4700 PF)  
FC\_HPF, WOOFERS = ~4 HZ (1.0 UF)

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

SYNC MASTER=J16 DIRK

SYNC DATE=03/07/2013

AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP  
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB  
SPEAKER AMP RIN = 40K NOMINAL  
FC\_HPFF, TWEETERS = ~847 HZ (4700 PF)  
FC\_HPFF, WOOFERS = ~4 HZ (1.0 UF)

D

D

C

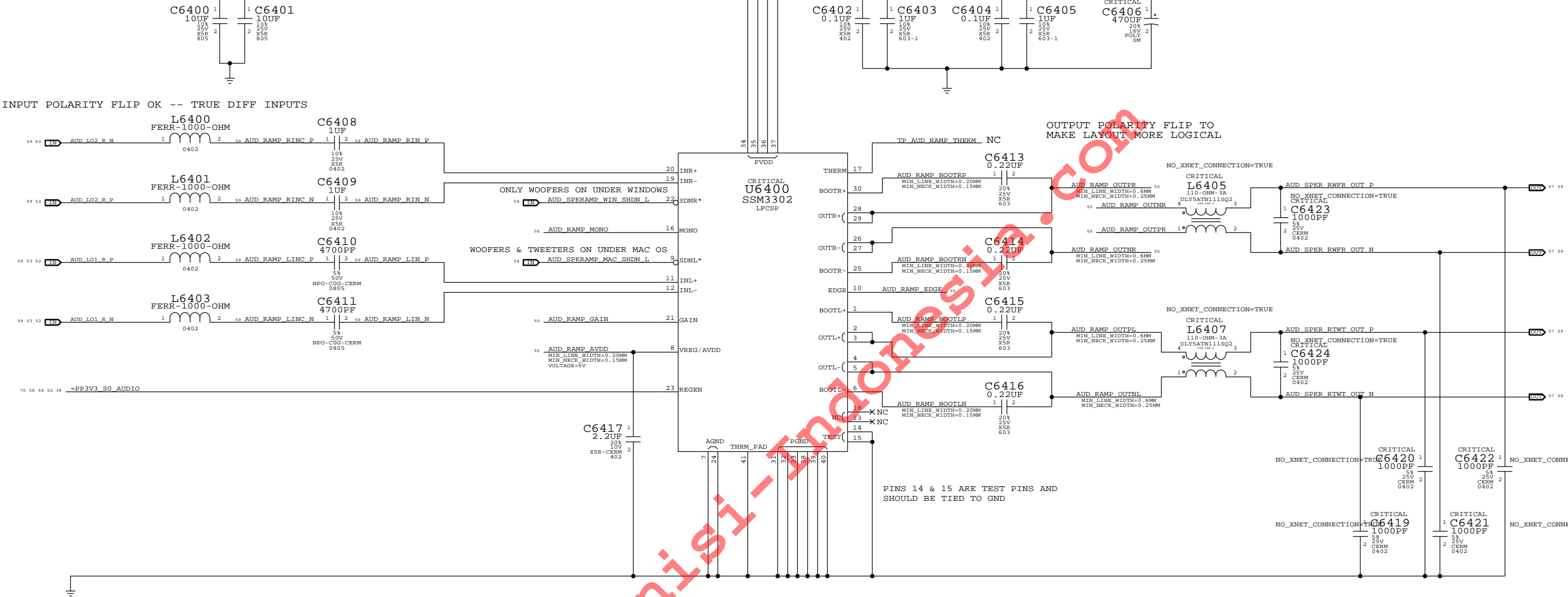
C

B

B

A

A



EDGE RATE CONTROL  
ON  
OFF

R6404  
0 OHM  
NOSTUFF

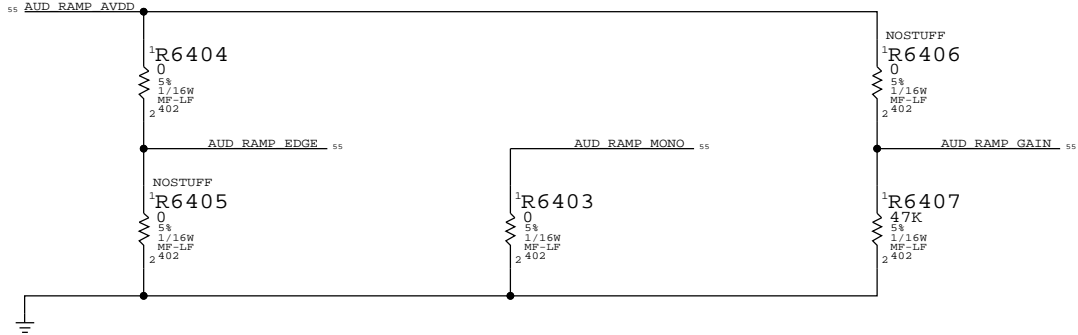
R6405  
NOSTUFF  
0 OHM


AUD\_RAMP\_MONO NET:  
HIGH = MONO OPERATION  
LOW = STEREO OPERATION

GAIN  
+9 DB  
+12 DB  
+15 DB  
+18 DB  
+24 DB

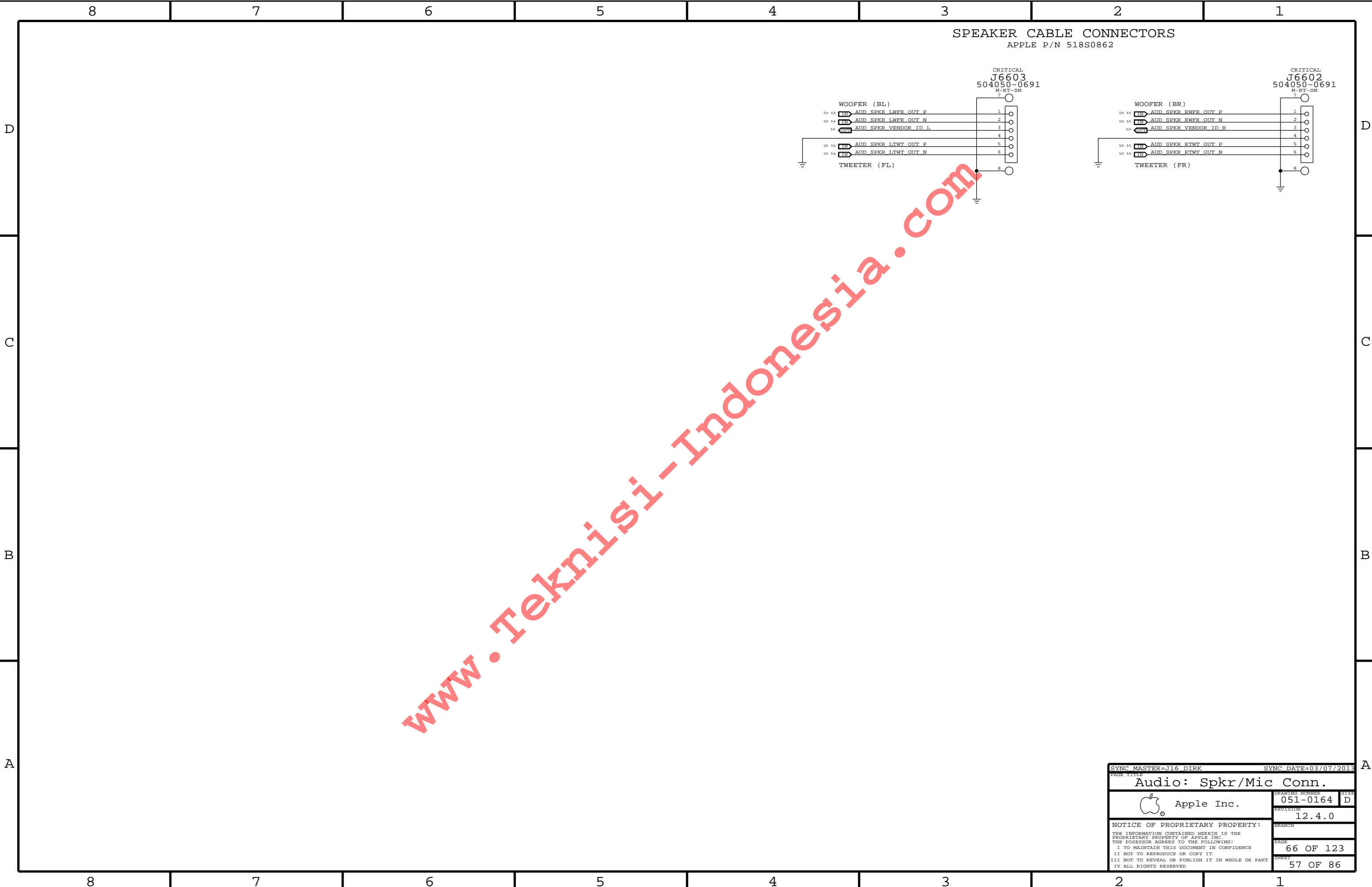
R6406  
NOSTUFF  
NOSTUFF  
47 KOHM  
0 OHM

R6407  
0 OHM  
47 KOHM  
NOSTUFF  
NOSTUFF

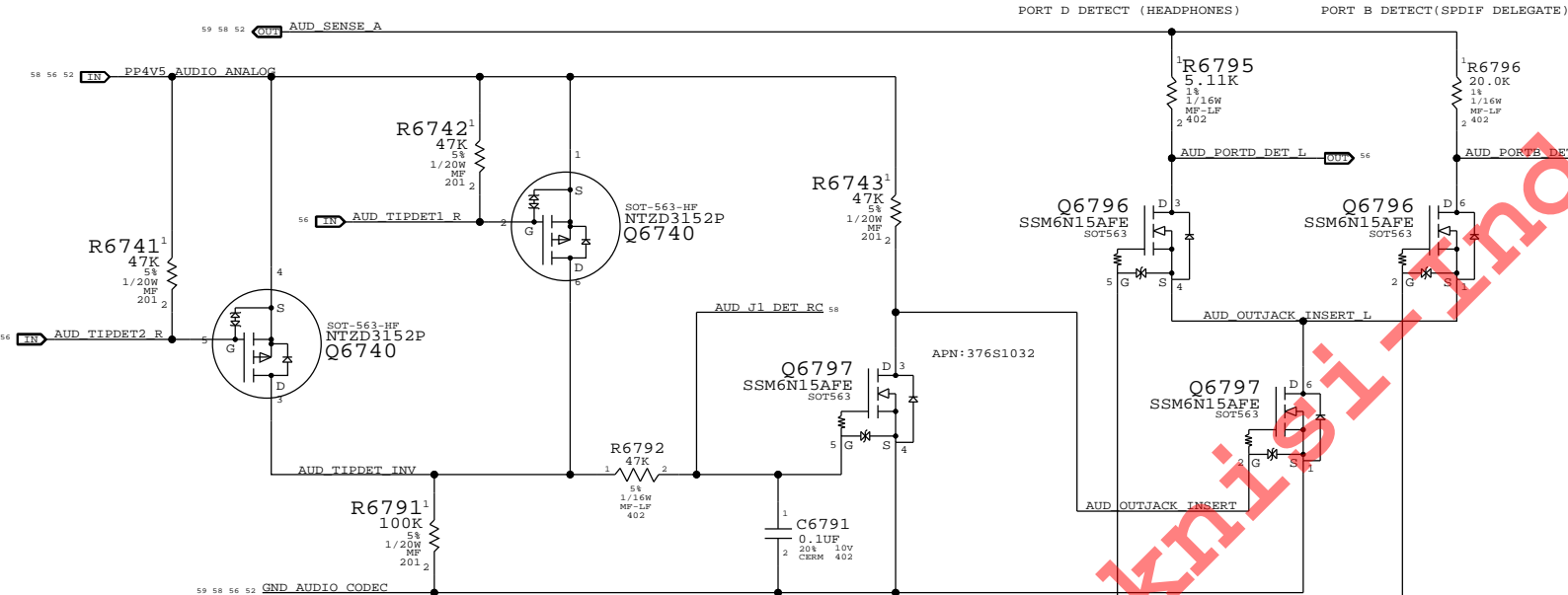
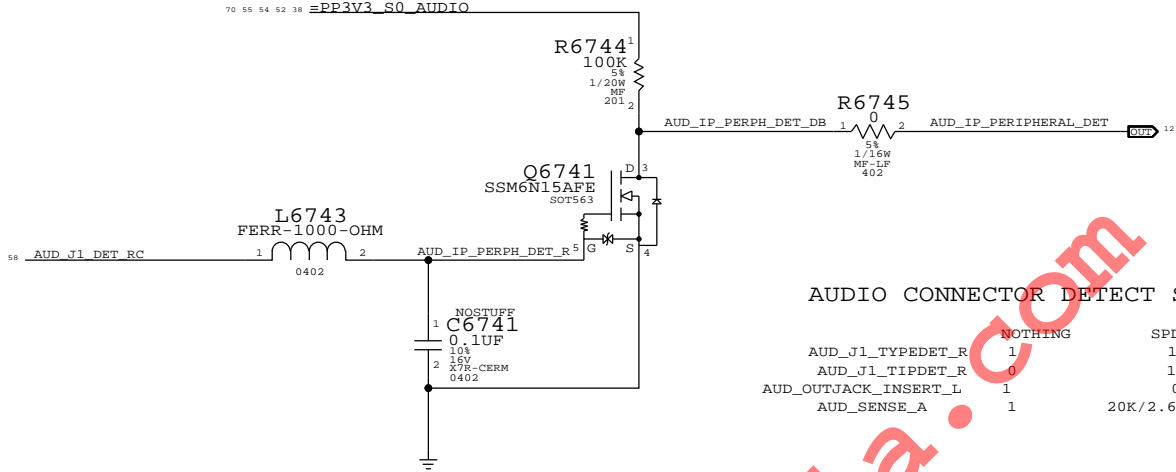


SYNC MASTER=J16 DIRK		SYNC DATE=03/07/2013	
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AUDIO: RIGHT SPKR AMP			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE
	REVISION	12.4.0	D
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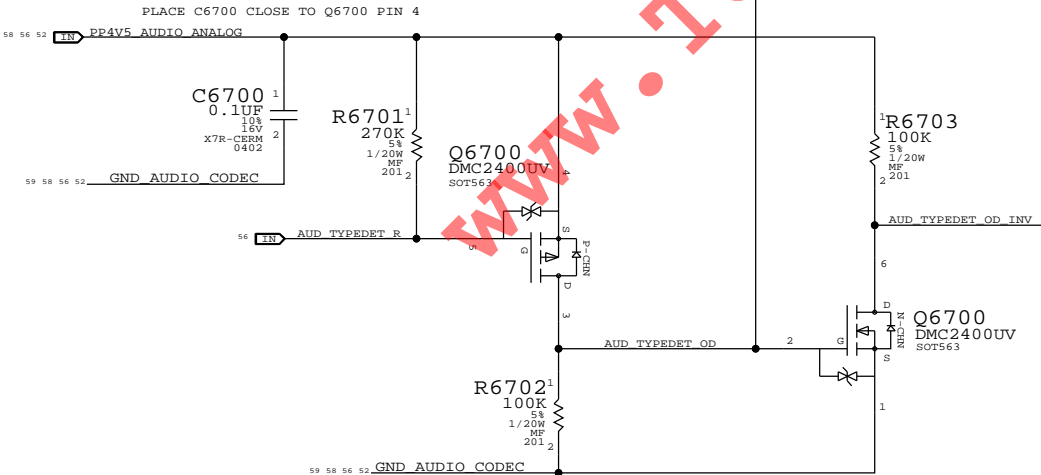
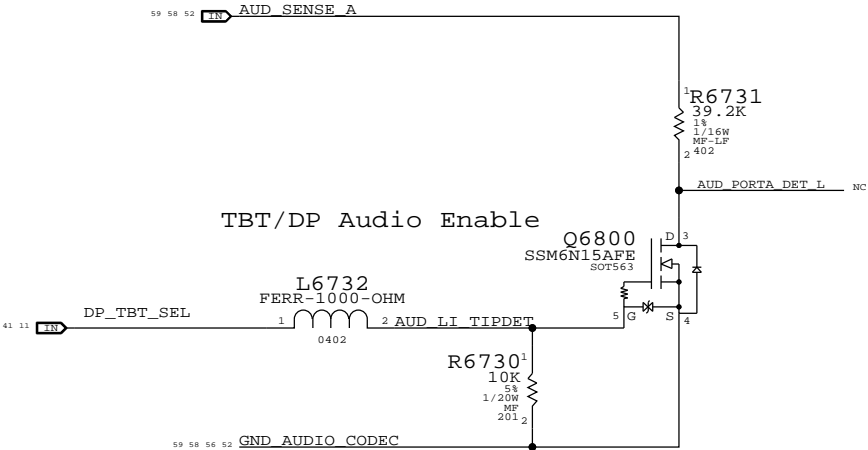




IPHS HS Detect Debounce CKT



Target Display Mode Detect





D  
C  
B  
A

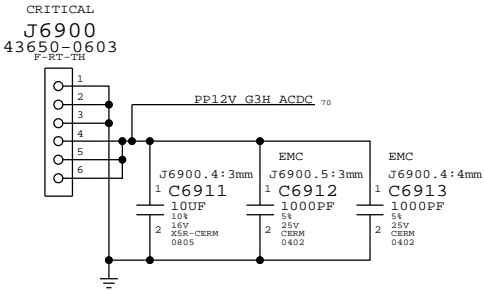
D  
C  
B  
A

3.425V "G3Hot" Regulator

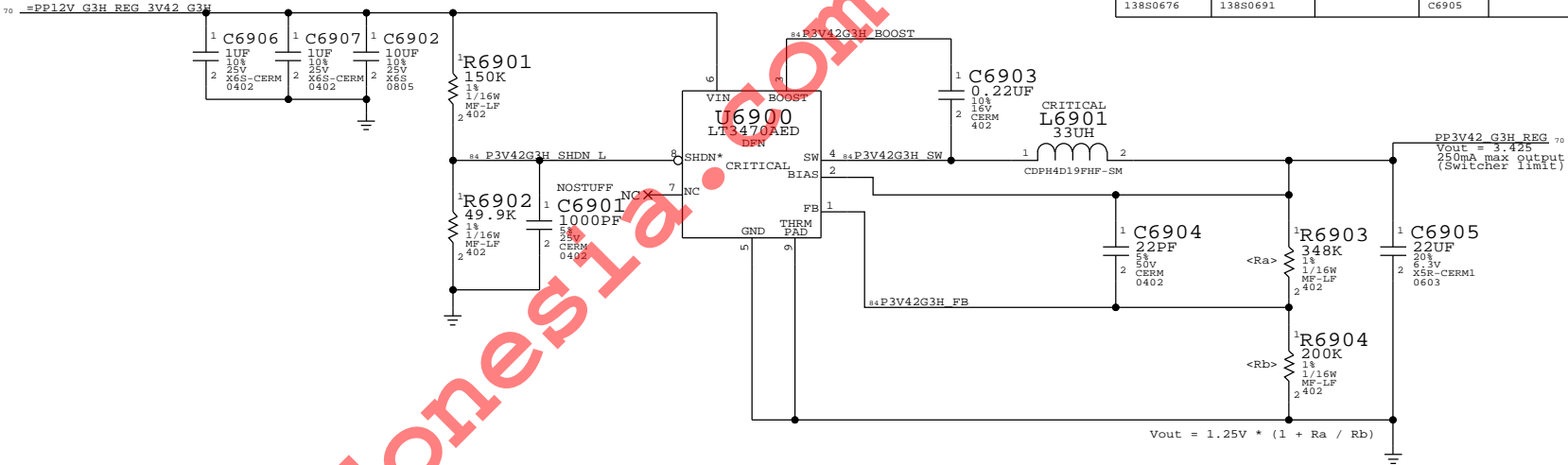
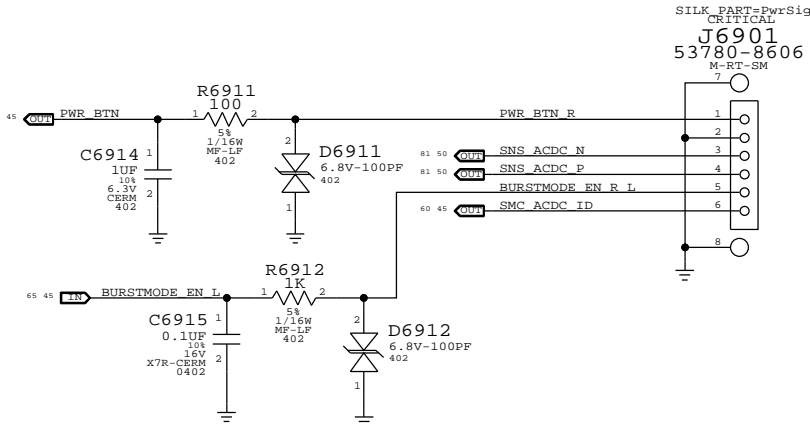
Switching freq: 409 kHz =  $\frac{13.5}{L6901}$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
138S0676	138S0691		C6905	

MLB to AC-DC Connector

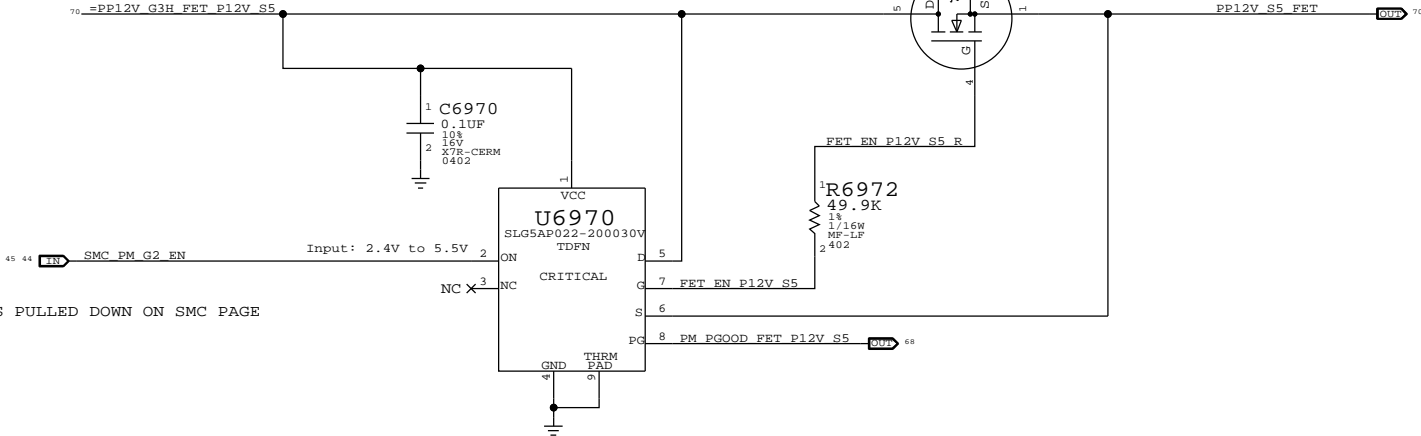



MLB to AC-DC Supplemental Signal Connector



12V S5 FET

SMC\_PM\_G2\_EN IS PULLED DOWN ON SMC PAGE



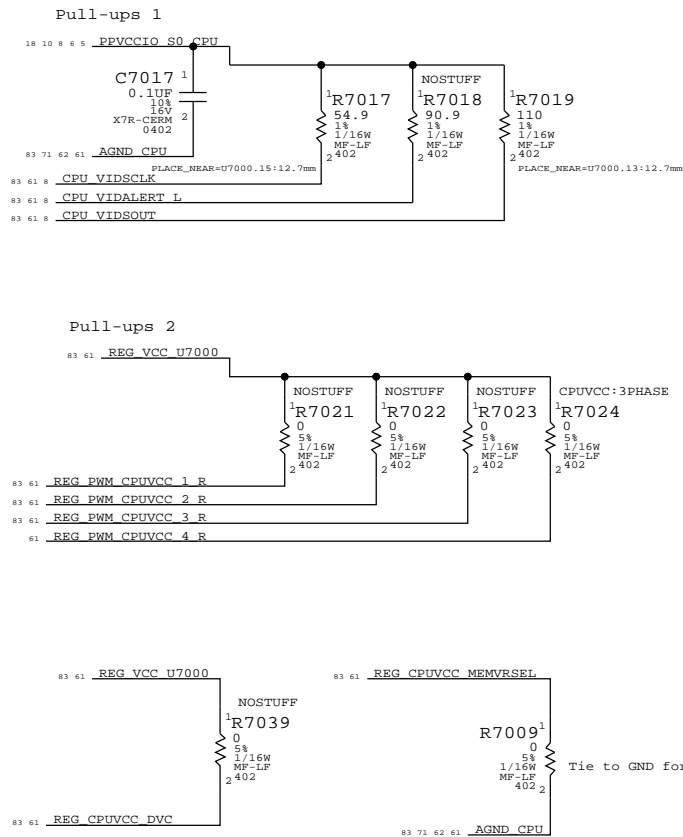
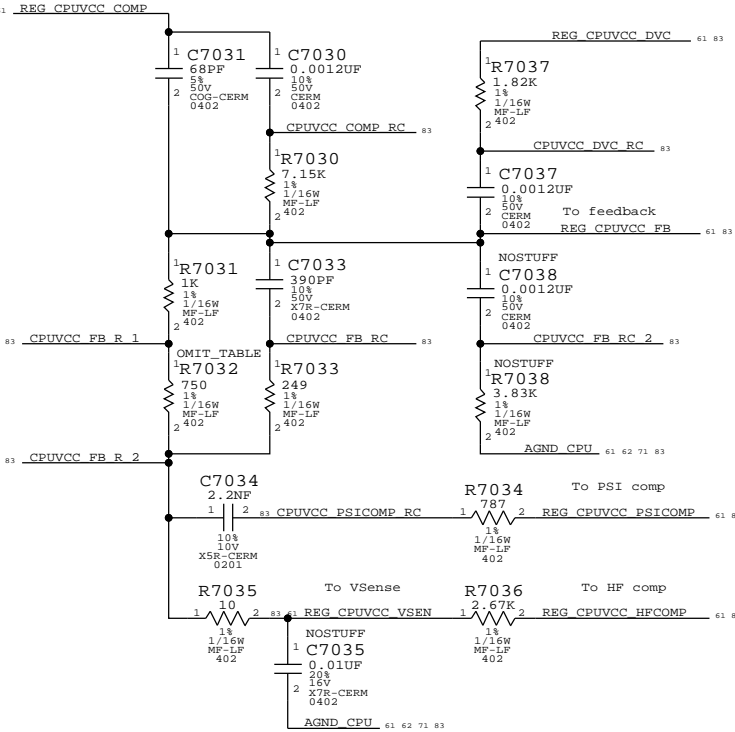
SYNC MASTER=J16 ROSSANA		SYNC DATE=03/04/2013	
PAGE TITLE			
Power Connectors / VReg G3Hot			
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		REVISION	12.4.0
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CPU VCC S0 Regulator

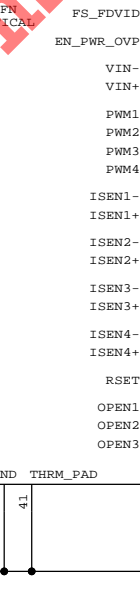
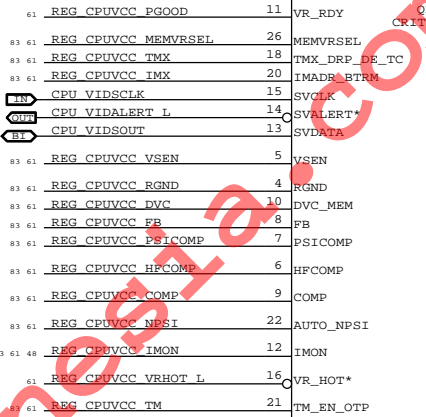
OC trip point: 114 A

Switching freq: 403 kHz =  $\frac{5}{R7003}$

Compensation and feedback

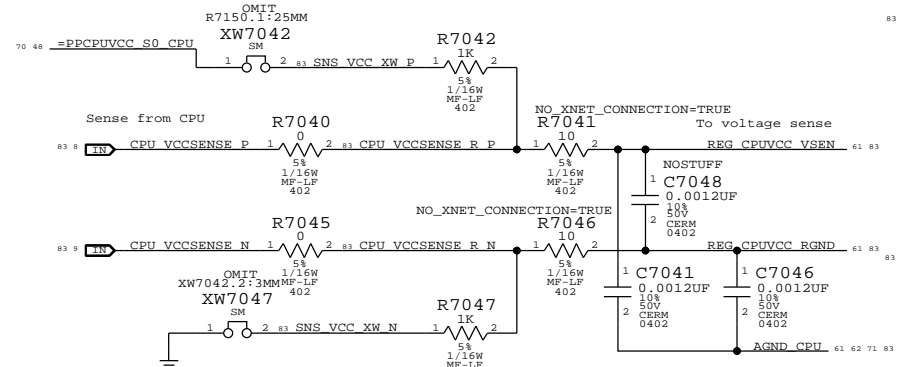


(pgood)  
(straps)  
(pu 1)  
(pu 1)  
(vsn in)  
(fb in)  
(psi comp)  
(hf comp)  
(comp out)  
(straps)  
(imon out)  
(vr hot out)

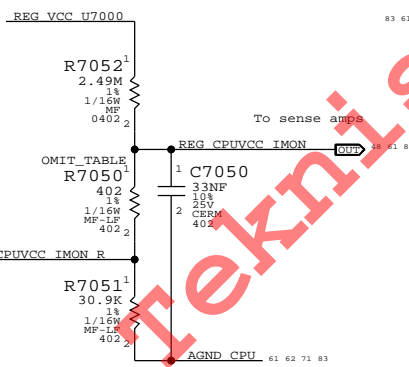


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480324	1	RES,12.7K,402	R7016	CPUVCC:3PHASE
11480316	1	RES,10.2K,402	R7016	CPUVCC:4PHASE

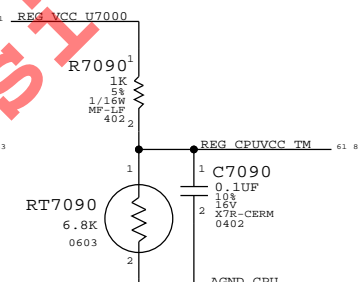
Voltage sense input



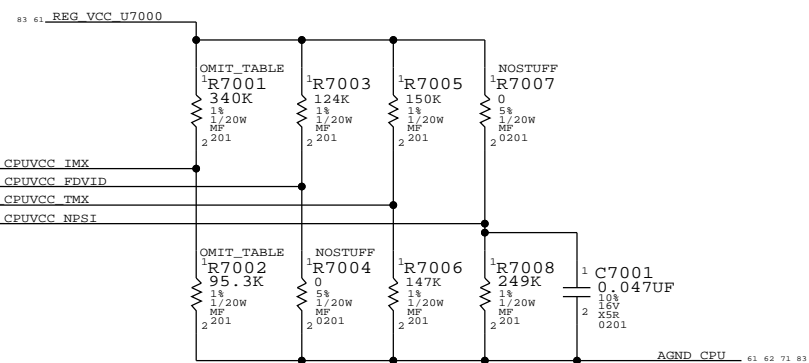
IMON output



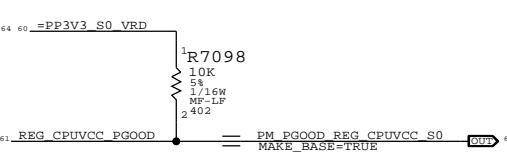
Temp measurement



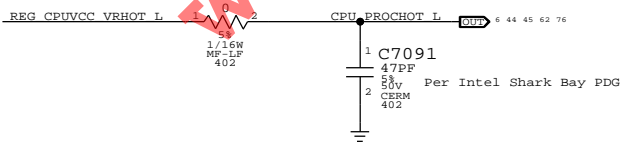
Straps



Power goods

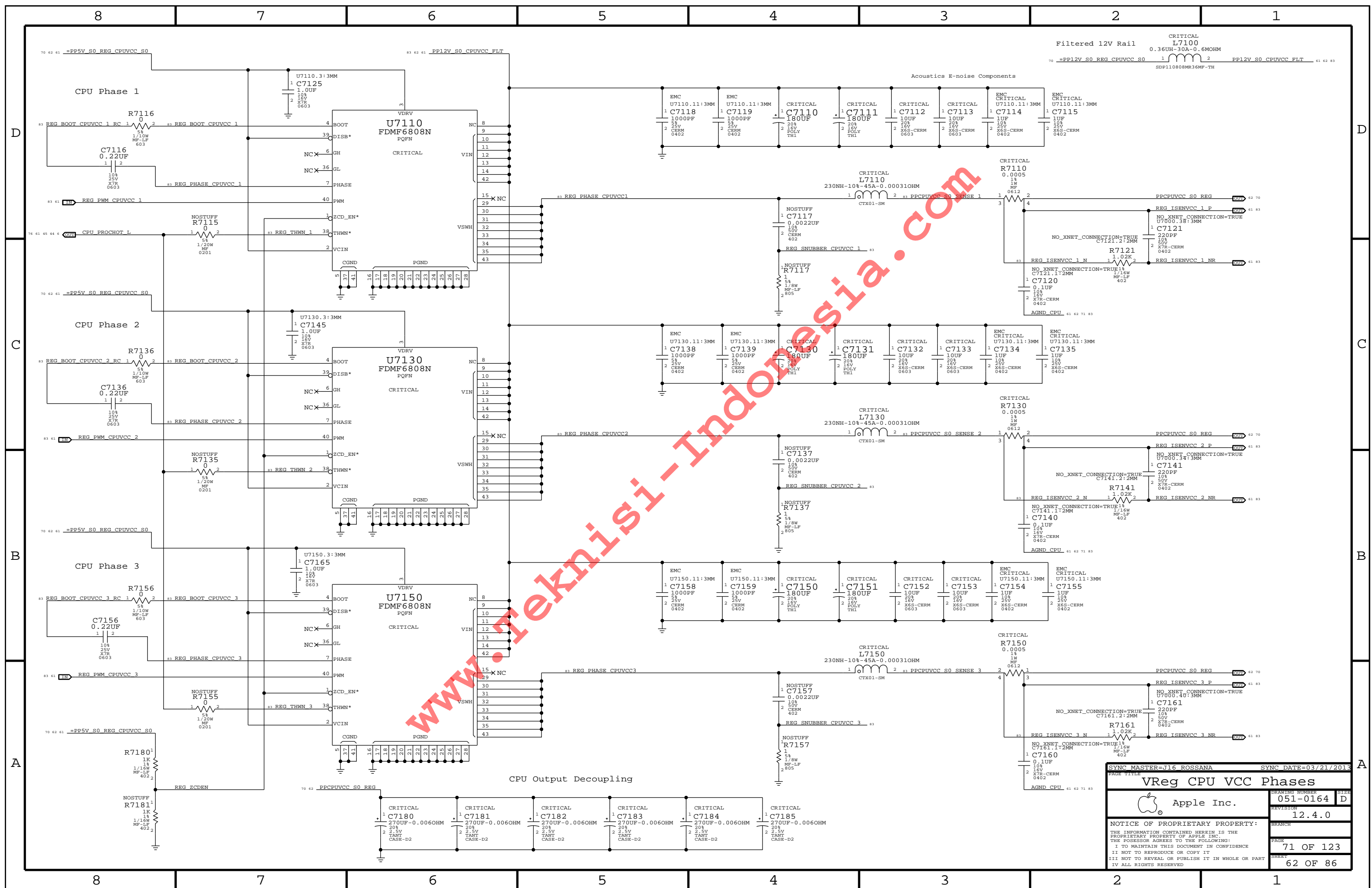


VRHot to ProcHot



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11880311	1	RES,340K,201	R7001	CPUVCC:3PHASE
11880116	1	RES,158K,201	R7001	CPUVCC:4PHASE
11880575	1	RES,95.3K,201	R7002	CPUVCC:3PHASE
11880380	1	RES,44.2K,201	R7002	CPUVCC:4PHASE
11480206	1	RES,750 OHM,402	R7032	CPUVCC:3PHASE
11480211	1	RES,845 OHM,402	R7032	CPUVCC:4PHASE
11480179	1	RES,402 OHM,402	R7050	CPUVCC:3PHASE
11480184	1	RES,453 OHM,402	R7050	CPUVCC:4PHASE

SYNC MASTER=J16 ROSSANA		SYNC DATE=03/21/2013	
PAGE TITLE			
VReg CPU VCC Cntl			
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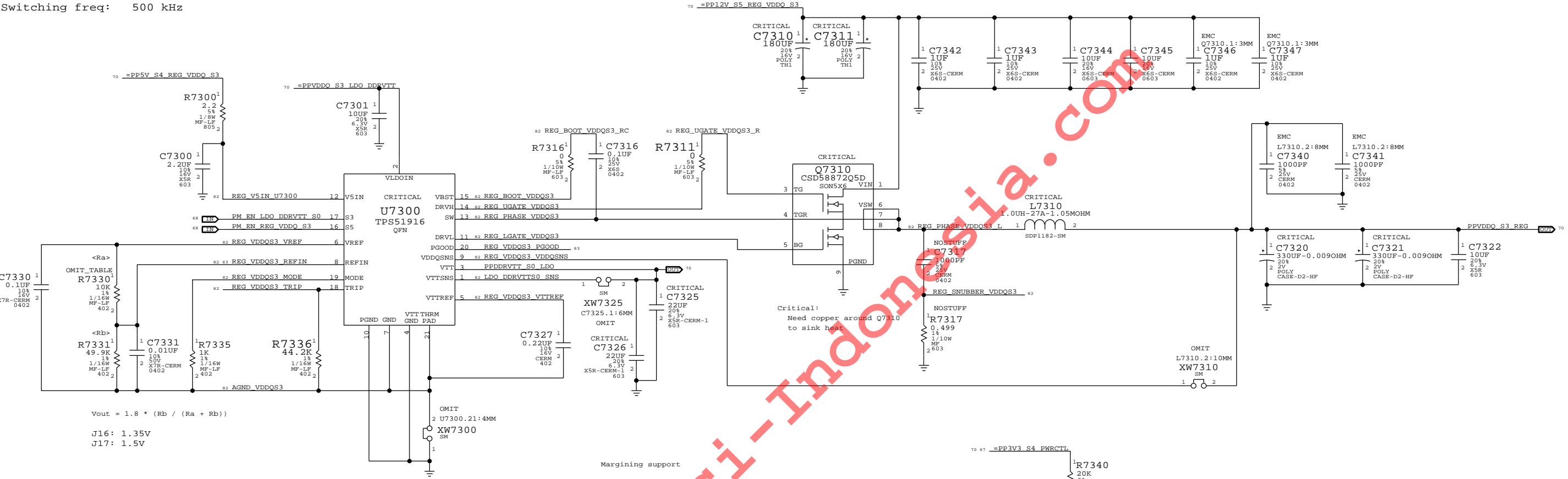


VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point:  $30.4 \text{ A VDDQ} = \frac{R7336}{8 \text{ E5} * R_{ds}(Q7310)} + \frac{0.65625}{L7310 * f(\text{switch})}$

3 A VTT (FIXED)  
10 mA VTTREF (FIXED)

Switching freq: 500 kHz

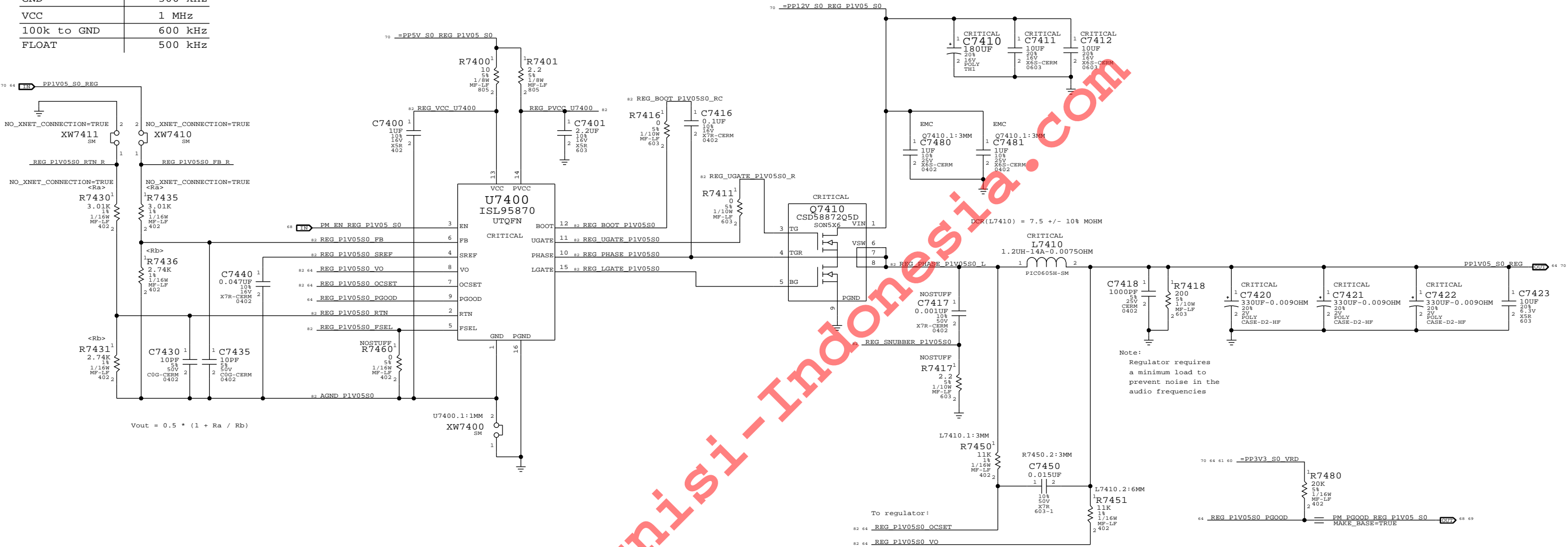


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480335	1	RES,16.5K,402	R7330	VDDQ:P1V35
11480315	1	RES,10K,402	R7330	VDDQ:P1V5

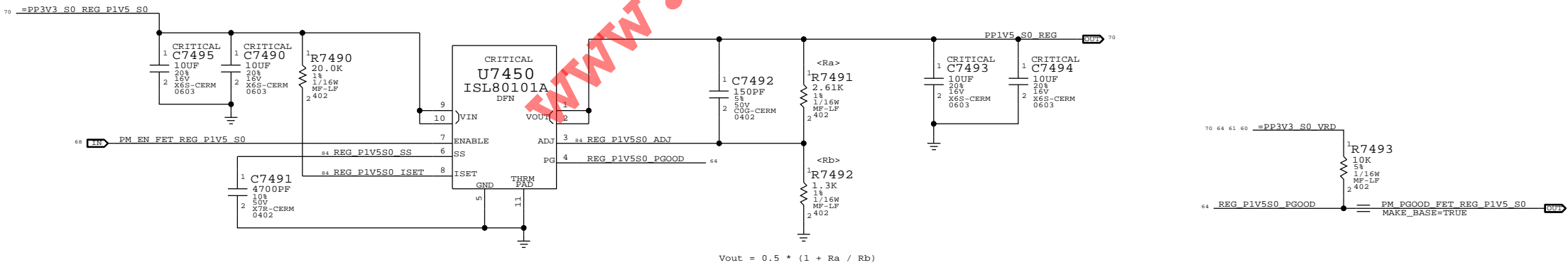
PCH/TBT (1.05V) S0 REGULATOR

Switching freq: 500 kHz    OC trip point: 12.4 A =  $\frac{R7450 \cdot 8.5 \cdot 10^{-6}}{DCR(L7410)}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



1.5V S0 REGULATOR



SYNC MASTER=J16 ROSSANA		SYNC DATE=03/04/2013	
PAGE TITLE		VREG 1V05 S0 / 1V5 S0	
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### 3.3V S5 Regulator

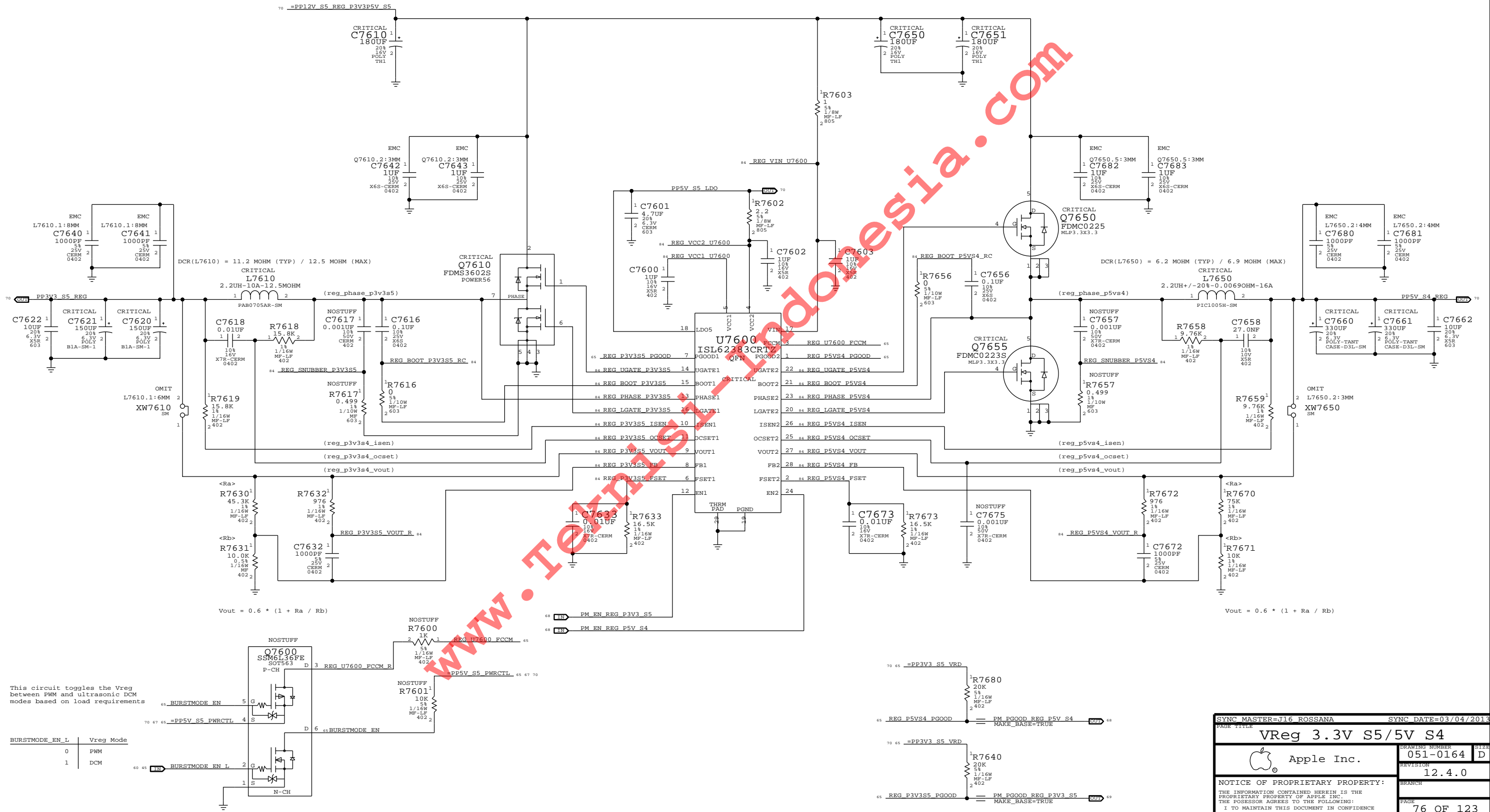
OC trip point:  $12.5 \text{ A} = \frac{R7618 * 10 \text{ E-6}}{\text{DCR}(L7610)}$

Switching freq:  $356 \text{ kHz} = \frac{1}{170 \text{ E-12} * R7633}$

### 5V S4 Regulator


OC trip point:  $14.1 \text{ A} = \frac{R7658 * 10 \text{ E-6}}{\text{DCR}(L7650)}$

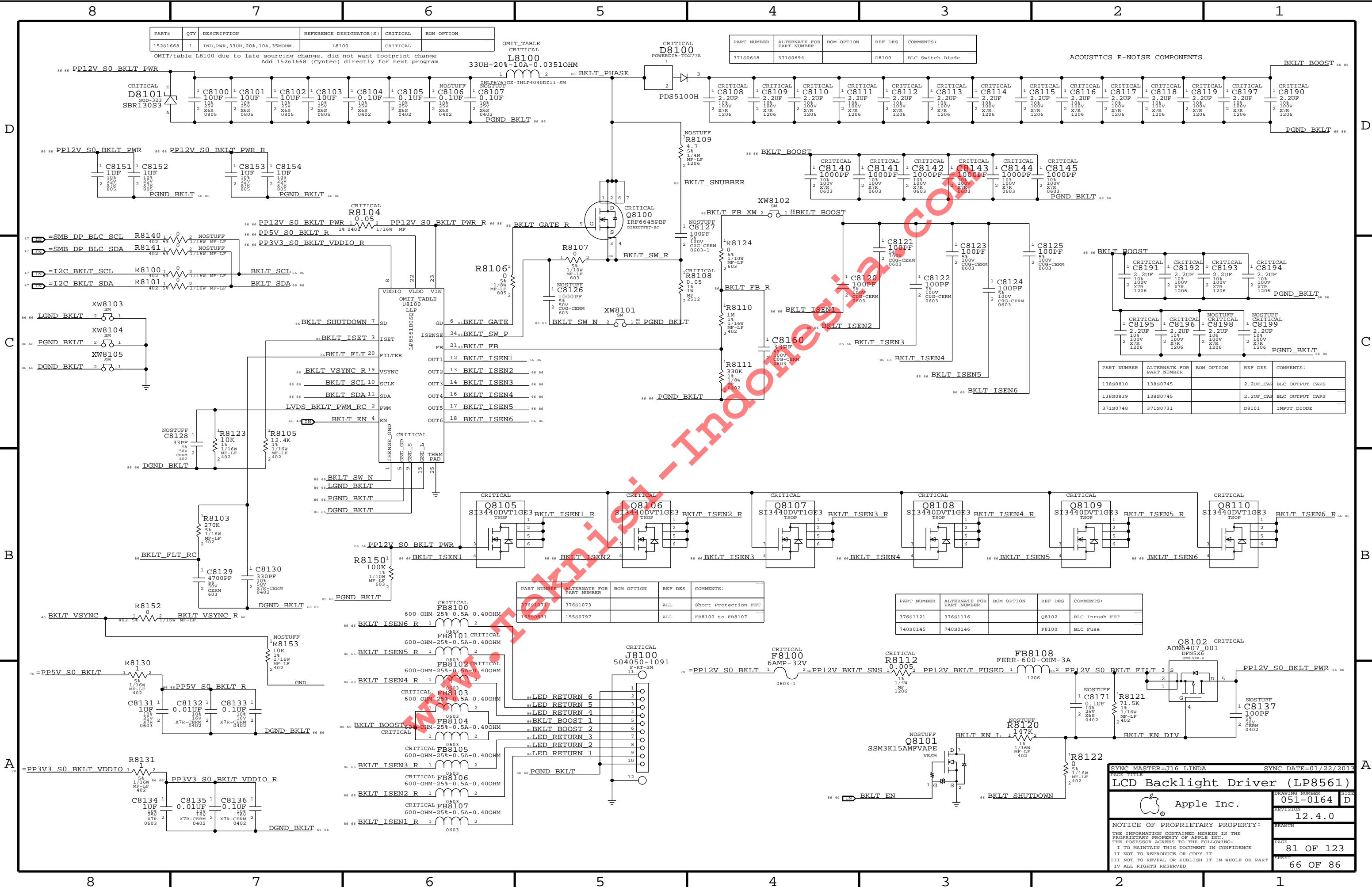
Switching freq:  $356 \text{ kHz} = \frac{1}{170 \text{ E-12} * R7673}$



This circuit toggles the Vreg between PWM and ultrasonic DCM modes based on load requirements

BURSTMODE_EN_L	Vreg Mode
0	PWM
1	DCM

SYNC MASTER=J16 ROSSANA		SYNC DATE=03/04/2013	
PAGE TITLE			
VReg 3.3V S5/5V S4			
 Apple Inc.	DRAWING NUMBER	051-0164	SIZE D
	REVISION	12.4.0	
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PAGE		76 OF 123	
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
-------	-----	-------------	-------------------------	----------	------------

OMIT/table L8100 due to late sourcing change, did not want footprint change  
Add 152s1668 (Cyntec) directly for next program

CRITICAL  
L8100  
33UH-20%-10A-0.03510HM

CRITICAL  
D8100  
POWERD15-T0277A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	---------------------------	------------	---------	-----------

ACOUSTICS E-NOISE COMPONENTS

BKLT BOOST

PGND BKLT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0810	138S0745		2.2UF_CAP	BLC OUTPUT CAPS
138S0839	138S0745		2.2UF_CAP	BLC OUTPUT CAPS
371S0748	371S0731		D8101	INPUT DIODE

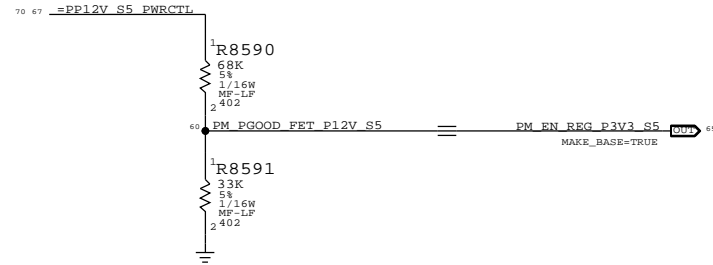
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

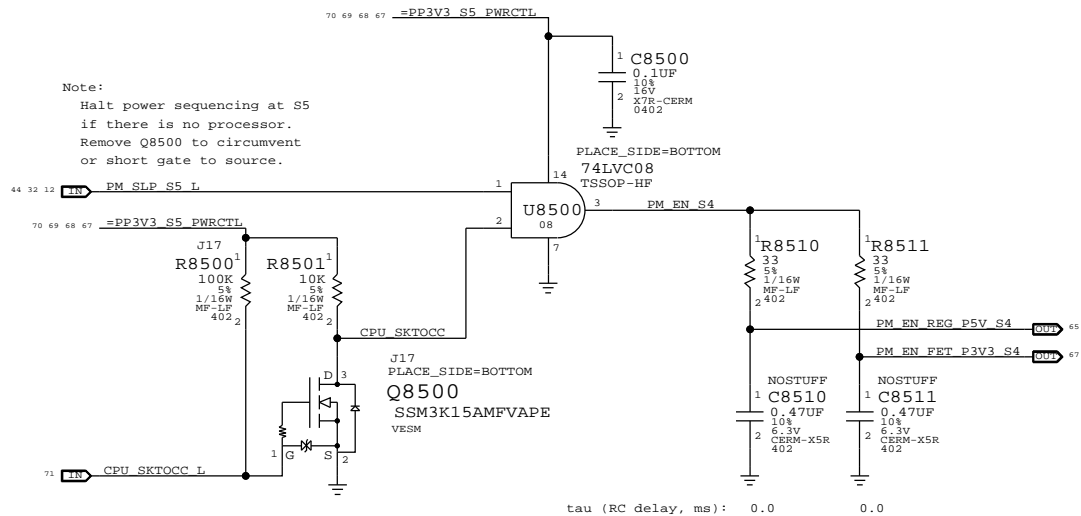
SYNC MASTER=J16 LINDA		SYNC DATE=01/22/2013	
PAGE TITLE		DRAWING NUMBER	
LCD Backlight Driver (LP8561)		051-0164	
Apple Inc.		REVISION	
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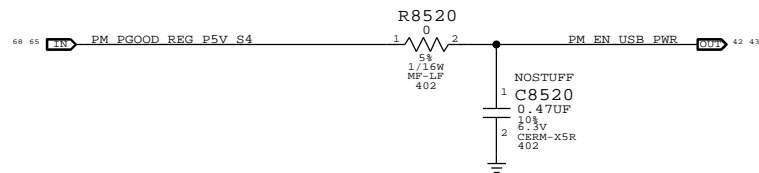
## S5 Enable



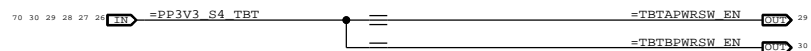
## S4 Enables



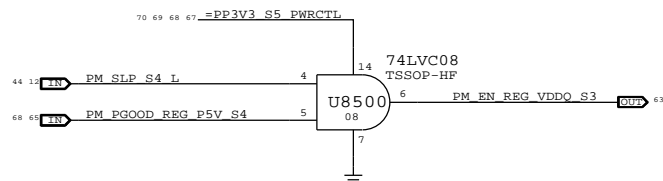
## S4 USB Enable



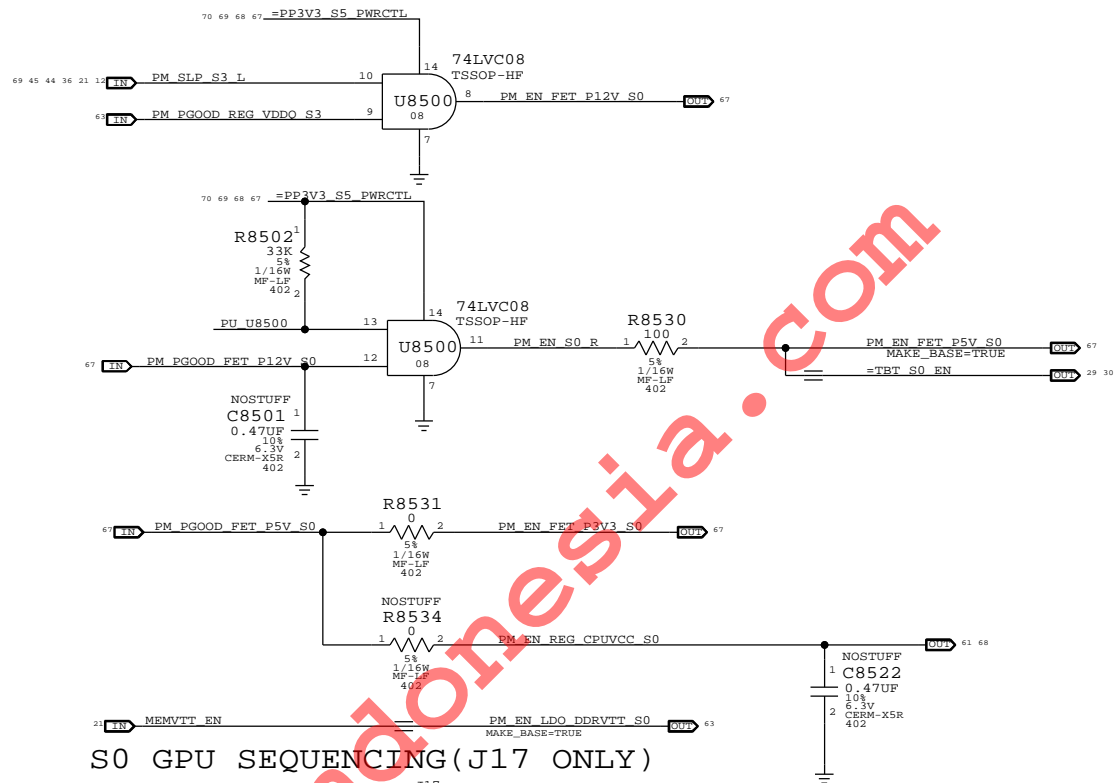
## S4 TBT S4 Port Enable



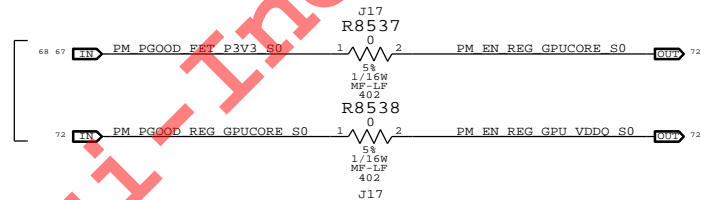
## S3 VDDQ Enable



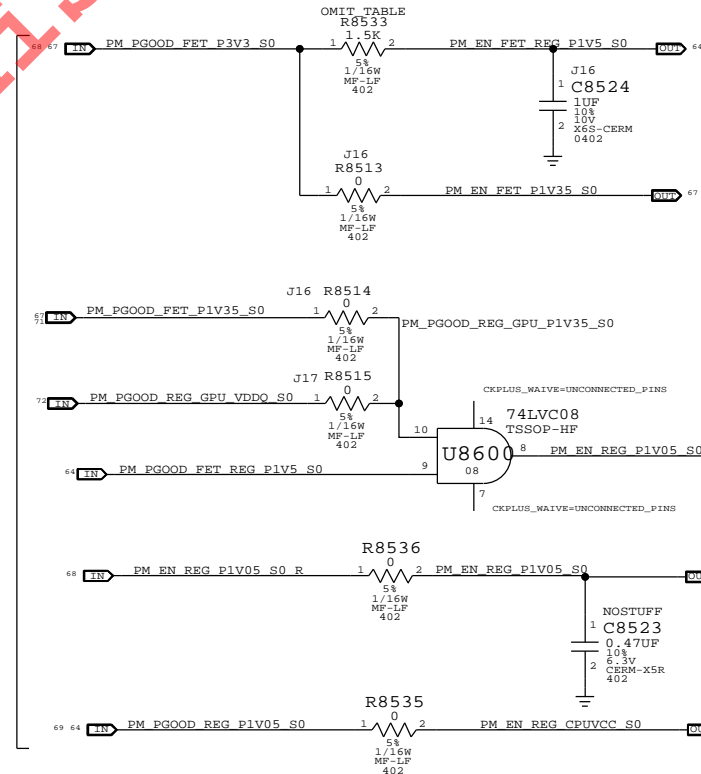
## S0 Enables



## S0 GPU SEQUENCING (J17 ONLY)



## S0 PCH Sequencing




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0070	1	RES,1.5K,0402,5%	R8533	J16
116S0004	1	RES,00HM,0402,5%	R8533	J17

### Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)  
Uncore: VDDQ

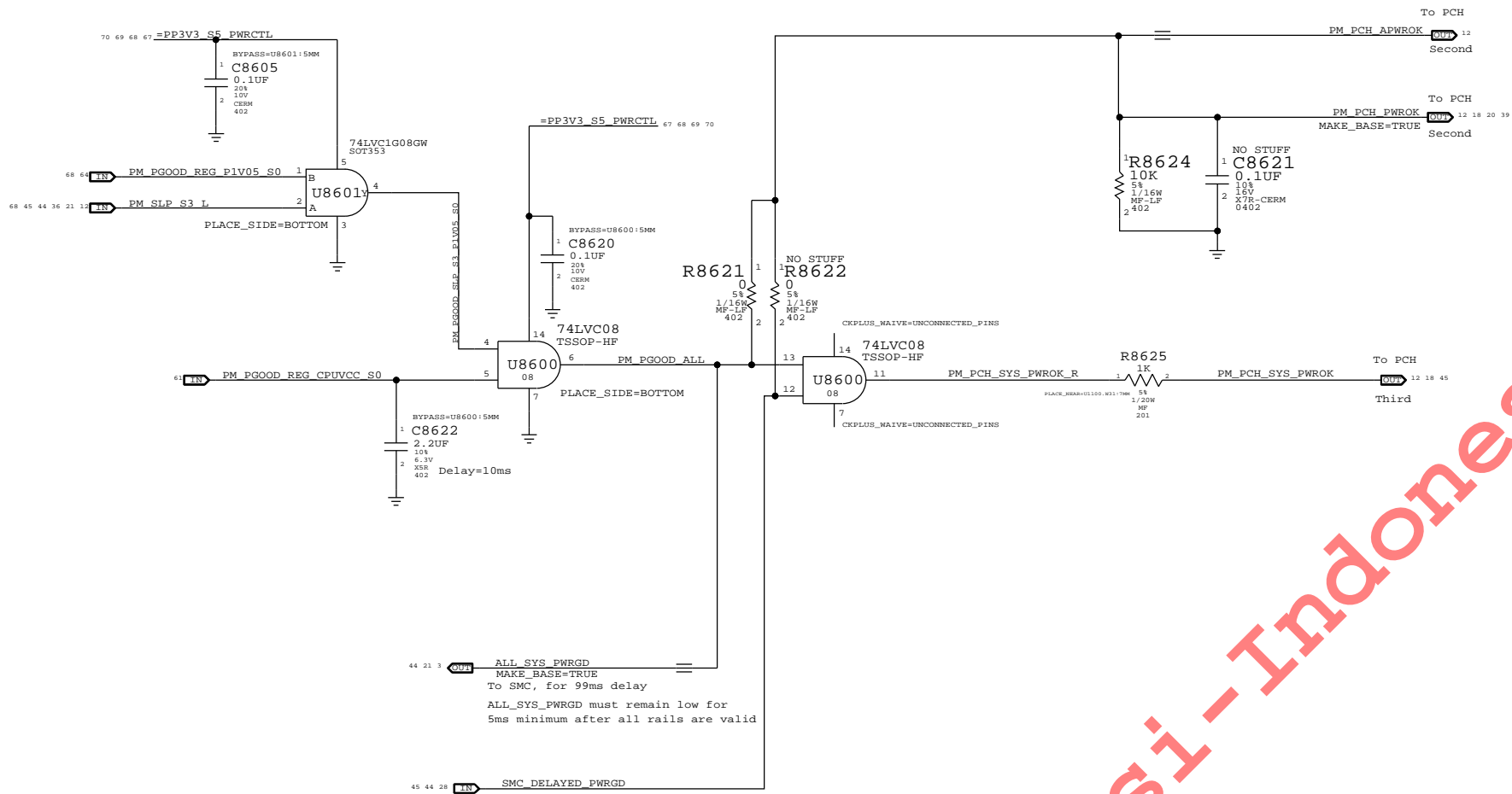
### Notes on sequencing requirements

- Intel:
- No hard specification on platform rails
  - SMC guarantees timing on PCH DPWROK and PWROK
  - VCC3\_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
  - VCC1\_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
  - VCC may power down before VCC3\_3, VCC3\_3 must ramp down to 2.6V within 35ms
  - VCC may power down before VCC1\_5, VCC1\_5 must ramp down to 1.35V within 35ms
- NVIDIA:
- 3V3\_S0 must ramp first
  - VDDQ MUST RAMP AFTER GPU\_CORE
  - PEX\_VDD with IFPC/D/E/F\_IOVDD (1.05V) must ramp after VDDQ
  - All rails must reach their target voltages in more than 40 uS

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PM Regulator Enables			
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ALL\_SYS\_PWRGD,PCH\_PWROK & SYS\_PWROK Generation

PCH Power Goods

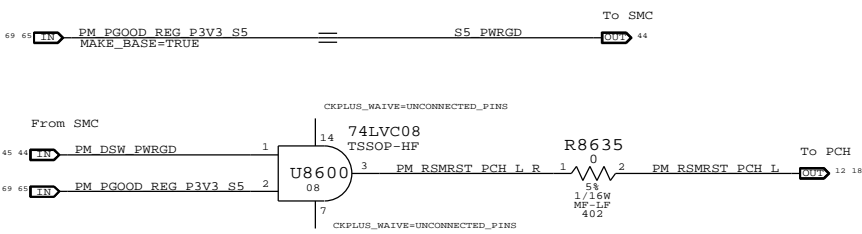


Resume Reset

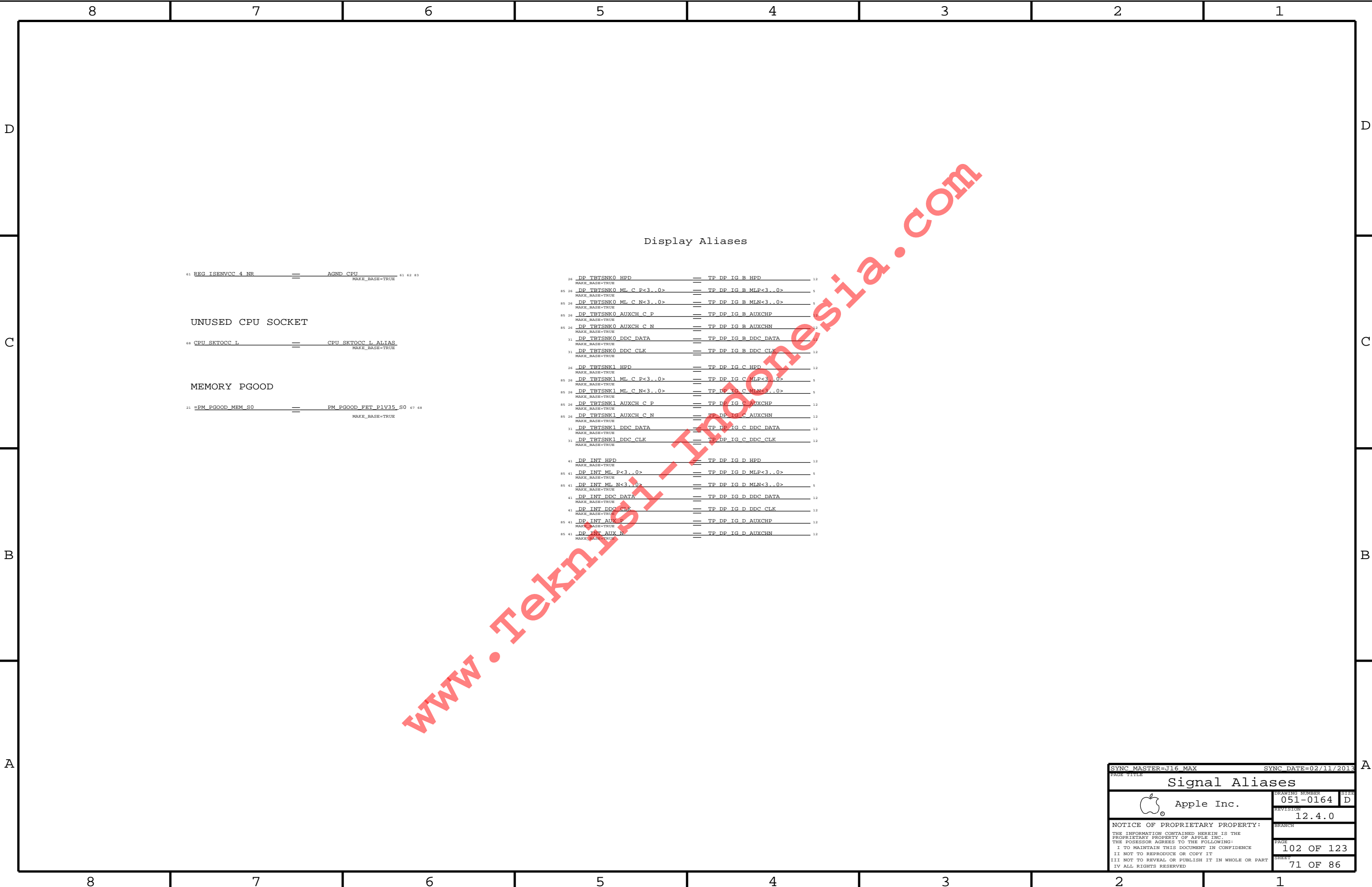
Intel Doc# 29517 Maho Bay PDG, Section 22.13  
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8  
Note:  
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:  
Power on:  
Asserted at least 10 ms after all suspend well power is valid  
Power off or loss of AC:  
Transition to 0.8V or less before VccSUS3\_3 drops to 2.90 V  
to allow PCH to switch suspend well to battery without excessive loading

Method:  
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM\_DSW\_PWRGD.  
RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.








8	7	6	5	4	3	2	1
CPU Reserved		UNUSED GRAPHICS ALIASES					
78 18 6 CPU CFG<15..12> == TP_CPU_CFG<15..12> MAKE_BASE=TRUE		20 TP_GPU_RESET_L == NC_TP_GPU_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE					
CPU Memory		UNUSED THUNDERBOLT ALIASES					
75 MEM_A_CLK_N<2..3> == NC_MEM_A_CLKN<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESETO_L == NC_TBT_PCIE_RESETO_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CLK_P<2..3> == NC_MEM_A_CLKP<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET1_L == NC_TBT_PCIE_RESET1_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CS_L<2..3> == NC_MEM_A_CS_L<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET2_L == NC_TBT_PCIE_RESET2_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_CKE<2..3> == NC_MEM_A_CKE<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_PCIE_RESET3_L == NC_TBT_PCIE_RESET3_L MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CLK_N<2..3> == NC_MEM_B_CLKN<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		26 TP_TBT_THERM_DP == NC_TBT_THERM_DP MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CLK_P<2..3> == NC_MEM_B_CLKP<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED VREG ALIASES					
75 MEM_B_CS_L<2..3> == NC_MEM_B_CS_L<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		61 REG_PWM_CPUVCC_4 == NC_REG_PWM_CPUVCC_4 MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_B_CKE<2..3> == NC_MEM_B_CKE<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		61 REG_ISENVCC_4_P == NC_REG_ISENVCC_4_P MAKE_BASE=TRUE NO_TEST=TRUE					
75 MEM_A_ODT<2..3> == NC_MEM_A_ODT<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED GPU ALIASES					
75 MEM_B_ODT<2..3> == NC_MEM_B_ODT<2..3> MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_EN_REG_GPUCORE_S0 == NC_PM_EN_REG_GPUCORE_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
PCH GPIO		68 PM_PGOOD_REG_GPUCORE_S0 == NC_PM_PGOOD_REG_GPUCORE_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO64_CLKOUTFLEX0 == NC_PCH_GPIO64_CLKOUTFLEX0 MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_EN_REG_GPU_VDDQ_S0 == NC_PM_EN_REG_GPU_VDDQ_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO65_CLKOUTFLEX1 == NC_PCH_GPIO65_CLKOUTFLEX1 MAKE_BASE=TRUE NO_TEST=TRUE		68 PM_PGOOD_REG_GPU_VDDQ_S0 == NC_PM_PGOOD_REG_GPU_VDDQ_S0 MAKE_BASE=TRUE NO_TEST=TRUE					
11 TP_PCH_GPIO66_CLKOUTFLEX2 == NC_PCH_GPIO66_CLKOUTFLEX2 MAKE_BASE=TRUE NO_TEST=TRUE		UNUSED PEG ALIASES					
11 TP_PCH_GPIO67_CLKOUTFLEX3 == NC_PCH_GPIO67_CLKOUTFLEX3 MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_D2R_P<0..15> == NC_PEG_D2R_P<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
UNUSED IG DISPLAY		5 =PEG_D2R_N<0..15> == NC_PEG_D2R_N<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_MLP<3..0> == NC_DP_IG_A_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_R2D_C_P<0..15> == NC_PEG_R2D_C_P<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_MLN<3..0> == NC_DP_IG_A_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE		5 =PEG_R2D_C_N<0..15> == NC_PEG_R2D_C_N<0..15> MAKE_BASE=TRUE NO_TEST=TRUE					
5 TP_DP_IG_A_AUXCHP == NC_DP_IG_A_AUXCHP MAKE_BASE=TRUE NO_TEST=TRUE		PCH PCI					
5 TP_DP_IG_A_AUXCHN == NC_DP_IG_A_AUXCHN MAKE_BASE=TRUE NO_TEST=TRUE		13 TP_LPC_DREQ0_L == NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE					
PCH Miscellaneous							
11 TP_HDA_SDIN1 == NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_HDA_SDIN2 == NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_HDA_SDIN3 == NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_PCI_CLK33M_OUT2 == NC_PCI_CLK33M_OUT2 MAKE_BASE=TRUE NO_TEST=TRUE							
11 TP_PCI_CLK33M_OUT3 == NC_PCI_CLK33M_OUT3 MAKE_BASE=TRUE NO_TEST=TRUE							
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## J16 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA	MM	16.2

## General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

## General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

### Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

## BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

## Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

## BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

## Board Stack-up

Finished board thickness: 1.58 mm

Layer	Material	Thickness
Top	Signal	0.5 oz (Cu plated)
	Prepreg	0.071 mm
2	Plane	1 oz
	Prepreg	0.076 mm
3	Signal	0.5 oz
	Prepreg	0.435 mm
4	Plane	1 oz
	Core	0.127 mm
5	Plane	1 oz
	Prepreg	0.435 mm
6	Signal	0.5 oz
	Prepreg	0.076 mm
2	Plane	1 oz
	Prepreg	0.071 mm
Btm	Signal	0.5 oz (Cu plated)



## PCI Express/DMI

## PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

## Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

## PCIE and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

## PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?
CPU_ASYNC_ISO	*	=3:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

## Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

## CPU ASYNCHRONOUS

Electrical Constraint Set	Physical	Spacing	
<b>ES00</b>	CEU_ASYNC_PHY	CEU_ASYNC	CPU PROCHOT_L 6 44 45 61 62
<b>ES01</b>	CEU_ASYNC_PHY	CEU_ASYNC	CPU PROCHOT_R_L 6
<b>ES02</b> PECE	CEU_ASYNC_PHY	CEU_ASYNC_MS	CPU PECE 6 14 44 45
<b>ES03</b>	CEU_ASYNC_PHY	CEU_ASYNC_MS	SMC PECE_L 44 45
<b>ES04</b>	CEU_ASYNC_PHY	CEU_ASYNC	CPU CATERR_L 6 45
<b>ES05</b>	CEU_ASYNC_PHY	CEU_ASYNC	CPU PWRGD 6 14 18
<b>ES06</b>	CEU_ASYNC_PHY	CEU_ASYNC	PM_SYNC 6 12
<b>ES07</b>	CEU_ASYNC_PHY	CEU_ASYNC	PM THRMTRIP_L 6 14 45
<b>ES08</b>	CEU_ASYNC_PHY	CEU_ASYNC	CPU RESET_L 6 14 18
<b>ES09</b> XDP_BPM_L	CEU_ASYNC_PHY	CEU_ASYNC	XDP BPM L<1..0> 6 18

## PCIe (CPU)

Electrical Constraint Set	Physical	Spacing	
CPU PCIe Compensation	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP
CPU eDP Compensation	COMP_EDP_PHY	COMP_EDP	CPU_EDP_RCOMP
	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIe Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIe Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIe Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCIe (PCH)

Electrical Constraint Set	Physical	Spacing
x4 Thunderbolt		
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
x1 AirPort		
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
x1 Caesar IV		
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_R2D	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_GEN2_D2R	PCIE_PHY	PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
x2 SSD		
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE
PCH PCIe Compensation		
COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP

CPU DP REF CLK

Electrical Constraint Set	Physical	Spacing
CPU DP REF CLK		
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE
CPU_CLK135_DLL	PCIE_PHY	CLK_PCIE

DMI

Electrical Constraint Set	Physical	Spacing
DMI		
DMI_N2S	PCIE_PHY	DMI_N2S
DMI_N2S	PCIE_PHY	DMI_N2S
DMI_S2N	PCIE_PHY	DMI_S2N
DMI_S2N	PCIE_PHY	DMI_S2N
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE
DMI Compensation		
COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP

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PCH PCIe/DMI Constaints			
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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?




Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO













SATA

Electrical Constraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
SATA_R2D	SATA_PHY_90	SATA	SATA HDD R2D P	33
SATA_R2D	SATA_PHY_90	SATA	SATA HDD R2D N	33
SATA_R2D	SATA_PHY_90	SATA	SATA HDD R2D C P	11 33
SATA_R2D	SATA_PHY_90	SATA	SATA HDD R2D C N	11 33
SATA_D2R	SATA_PHY_90	SATA	SATA HDD D2R P	11 33
SATA_D2R	SATA_PHY_90	SATA	SATA HDD D2R N	11 33
SATA_D2R	SATA_PHY_90	SATA	SATA HDD D2R C P	33
SATA_D2R	SATA_PHY_90	SATA	SATA HDD D2R C N	33
PCH SATA Port 1 (SSD)				
SATA_SSD_R2D	SATA_PHY	SATA	SSD R2D P<0..1>	11 33
SATA_SSD_R2D	SATA_PHY	SATA	SSD R2D N<0..1>	11 33
SATA_SSD_R2D	SATA_PHY	SATA	SSD R2D C P<0..1>	33
SATA_SSD_R2D	SATA_PHY	SATA	SSD R2D C N<0..1>	33
SATA_SSD_D2R	SATA_PHY	SATA	SSD D2R P<0..1>	11 33
SATA_SSD_D2R	SATA_PHY	SATA	SSD D2R N<0..1>	11 33
PCH SATA Compensation				
COMP_SATA_PHY	COMP_SATA_PHY	COMP_SATA	PCH SATA RCOMP	11

FDI

Electrical Constraint Set	Physical	Spacing		
FDI				
	FDI_SE_PHY	FDI	FDI CSYNC	5 12
	FDI_SE_PHY	FDI	FDI INT	5 12
FDI Compensation				
	COMP_FDI_PHY	COMP_FDI	PCH_FDI_RCOMP	12

XDP

Electrical Constraint Set		Physical	Spacing	
CPU XDP				
	XDP_BPM_1	XDP_PHY	XDP	XDP BPM L<7..2> 6 18
	XDP_CPU_CFG	XDP_PHY	XDP	CPU CFG<17..4> 6 18 72
	XDP_CPU_CFG_3	XDP_PHY	XDP	CPU CFG<3> 6 18
	XDP_CPU_CFG	XDP_PHY	XDP	CPU CFG<2..0> 6 18
		XDP_PHY	CLK_JTAG	XDP CPU TCK 6 18
		XDP_PHY	XDP	XDP CPU TMS 6 18
		XDP_PHY	XDP	XDP CPU TDI 6 18
		XDP_PHY	XDP	XDP CPU TDO 6 18
PCH XDP				
		XDP_PHY	CLK_JTAG	XDP PCH TCK 11 18
		XDP_PHY	XDP	XDP PCH TMS 11 18
		XDP_PHY	XDP	XDP PCH TDI 11 18
		XDP_PHY	XDP	XDP PCH TDO 11 18

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SATA/FDI/XDP Constraints

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## PCH

## PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

## PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

## PCI

## PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

## PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

## LPC

## LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

## LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

## HDA

## HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

## HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

## Crystal

### Crystal-specific Physical Rules

[illegible]

### Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

## SPI

## SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

## SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

## PCI

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Electrical Constraint Set	physical	spacing	
PCI Clock			
	CLK_PCT_55S	CLK_PCT	PCH_CLK33M_PCIIN 11 19
	CLK_PCT_55S	CLK_PCT	PCH_CLK33M_PCIOUT 11 19

## LPC

[illegible]

Electrical Constraint Set	Physical	Spacing	
LPC			
<b>R535</b>	LPC 55S	LPC	LPC AD<3...0> 13 44
<b>R536</b>	LPC 55S	LPC	LPC AD R<3...0> 13 44
<b>R537</b>	LPC 55S	LPC	LPC FRAME L 13 44
<b>R538</b>	LPC 55S	LPC	LPC FRAME R L 13 44
LPC Clocks			
<b>R539</b>	CLK LPC 55S	CLK LPC	LPC CLK33M LPCPLUS 11 19
<b>R540</b>	CLK LPC 55S	CLK LPC	LPC CLK33M LPCPLUS_R 11 19
<b>R541</b>	CLK LPC 55S	CLK LPC	LPC CLK33M SMC 11 19
<b>R542</b>	CLK LPC 55S	CLK LPC	LPC CLK33M SMC_R 11 19

## PCH Clocks

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...	...	...

Electrical Constraint Set	Physical	Spacing		
PCH Reference Clock				
<b>HS18</b>	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	11 19
<b>HS40</b>	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R	11
PCH RTC 32K				
<b>HS40</b>	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	11 19
<b>HS41</b>	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	11 19
<b>HS42</b>	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	19
SMC 32K				
<b>HS41</b>	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	12 45
<b>HS50</b>	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	44 45













25 MHz Reference Clocks

Elemental	Quantitative	Elemental	Quantitative
1	2	3	4

Electrical Constraint Set	Physical	Spacing		
25M Reference Crystal				
<b>REF1</b>	CLK XTAL	XTAL	SYSCLK CLK25M X1	19
<b>REF2</b>	CLK XTAL	XTAL	SYSCLK CLK25M X2	19
<b>REF3</b>	CLK XTAL	XTAL	SYSCLK CLK25M X2 R	19
25M Reference Clocks				
<b>REF4</b>	CLK PCH 55S	CLK PCH	SYSCLK CLK25M ENET	19 35
<b>REF5</b>	CLK PCH 55S	CLK PCH	SYSCLK CLK25M ENET R	19
<b>REF6</b>	CLK PCH 55S	CLK PCH	SYSCLK CLK25M TBT	19 26
<b>REF7</b>	CLK PCH 55S	CLK PCH	SYSCLK CLK25M TBT R	26

## HDA

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Electrical Constraint Set	Physical	Spacing	
HDA			
	HDA_55S	HDA	HDA BIT_CLK 11 92
	HDA_55S	HDA	HDA BIT_CLK_R 11 11
	HDA_55S	HDA	HDA RST_L 11 92
	HDA_55S	HDA	HDA RST_R_L 11 11
	HDA_55S	HDA	HDA SPDOUT 11 92
	HDA_55S	HDA	HDA SPDOUT_R 11 19
	HDA_55S	HDA	HDA SYNC 11 52
	HDA_55S	HDA	HDA SYNC_E 11 11
	HDA_55S	HDA	HDA SDIN0 11 52
	HDA_55S	HDA	AUD SDI_R 52
SPDIF			
		HDA	AUD SPDIF CHIP 52
		HDA	AUD SPDIF_OUT 52 56

## SPI Bootrom

Electrical Constraint Set	Physical	Creeping
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Electrical Constraint et		Physical	Spacing	
SPI ROM				
<b>E392</b>	SPI 50S	SPI	SPI CLK R	13 46
<b>E392</b>	SPI 50S	SPI	SPI CLK	46
<b>E393</b>	SPI 50S	SPI	SPI ALT CLK	46
<b>E400</b>	SPI 50S	SPI	SPI SMC CLK	44 46
<b>E400</b>	SPI 50S	SPI	SPI MLB CLK	46
<b>E392</b>	SPI 50S	SPI	SPI CS0 R L	13 46
<b>E393</b>	SPI 50S	SPI	SPI CS0 L	46
<b>E393</b>	SPI 50S	SPI	SPI ALT CS L	46
<b>E400</b>	SPI 50S	SPI	SPI SMC CS L	44 46
<b>E393</b>	SPI 50S	SPI	SPI MLB CS L	46
<b>E392</b>	SPI 50S	SPI	SPI MOSI R	13 46
<b>E400</b>	SPI 50S	SPI	SPI MOSI	46
<b>E400</b>	SPI 50S	SPI	SPI ALT MOSI	46
<b>E410</b>	SPI 50S	SPI	SPI SMC MOSI	44 46
<b>E410</b>	SPI 50S	SPI	SPI MLB MOSI	46
<b>E400</b>	SPI 50S	SPI	SPI MISO	13 46
<b>E410</b>	SPI 50S	SPI	SPI ALT MISO	46
<b>E410</b>	SPI 50S	SPI	SPI SMC MISO	44 46
<b>E410</b>	SPI 50S	SPI	SPI MLB MISO	46
<b>E400</b>	SPI 50S	SPI	SPIROM USE MLB	14 46

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Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

## Constraints Ethernet

NET_SPACING_TYP1	NET_SPACING_TYP2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF


Electrical Contract Set	Physical	Spacing	
<b>External Port A (J4600)</b>			
R577 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_A_RX_P 42
R580 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_A_RX_N 42
R579 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_RX_F_P 13 42
R582 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_RX_F_N 13 42
R583 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_A_TX_P 13 42
R584 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_A_TX_N 13 42
R586 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_TX_F_P 42
R588 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_TX_F_N 42
R589 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_TX_C_P 42
R590 USB3_PHV	USB3_PHV	USB3	USB3_EXT_A_TX_C_N 42
R591 USB2_MIXED_M0T0_CONN	USB2_PHV	USB2	USB_EXT_A_0_P 13 42
R592 USB2_MIXED_M0T0_CONN	USB2_PHV	USB2	USB_EXT_A_0_N 13 42
R593 USB2_PHV	USB2_PHV	USB2	USB2_EXT_A_MIXED_P 42
R594 USB2_PHV	USB2_PHV	USB2	USB2_EXT_A_MIXED_N 42
R595 USB2_PHV	USB2_PHV	USB2	USB2_EXT_A_P 42
R596 USB2_PHV	USB2_PHV	USB2	USB2_EXT_A_N 42
<b>External Port B (J4610)</b>			
R598 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_B_RX_P 42
R599 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_B_RX_N 42
R600 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_RX_F_P 13 42
R601 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_RX_F_N 13 42
R602 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_B_TX_P 13 42
R603 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_B_TX_N 13 42
R604 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_TX_F_P 42
R605 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_TX_F_N 42
R606 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_TX_C_P 42
R607 USB3_PHV	USB3_PHV	USB3	USB3_EXT_B_TX_C_N 42
R608 USB2_CONN	USB2_PHV	USB2	USB_EXT_B_8_P 13 42
R609 USB2_CONN	USB2_PHV	USB2	USB_EXT_B_8_N 13 42
R610 USB2_PHV	USB2_PHV	USB2	USB2_EXT_B_P 42
R611 USB2_PHV	USB2_PHV	USB2	USB2_EXT_B_N 42
<b>External Port C (J4700)</b>			
R613 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_C_RX_P 43
R614 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_C_RX_N 43
R615 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_RX_F_P 13 43
R616 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_RX_F_N 13 43
R617 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_C_TX_P 13 43
R618 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_C_TX_N 13 43
R619 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_TX_F_P 43
R620 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_TX_F_N 43
R621 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_TX_C_P 43
R622 USB3_PHV	USB3_PHV	USB3	USB3_EXT_C_TX_C_N 43
R623 USB2_CONN	USB2_PHV	USB2	USB_EXT_C_1_P 13 43
R624 USB2_CONN	USB2_PHV	USB2	USB_EXT_C_1_N 13 43
R625 USB2_PHV	USB2_PHV	USB2	USB2_EXT_C_P 43
R626 USB2_PHV	USB2_PHV	USB2	USB2_EXT_C_N 43
<b>External Port D (J4710)</b>			
R628 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_D_RX_P 43
R629 USB3_RX_CONN	USB3_PHV	USB3	USB3_EXT_D_RX_N 43
R630 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_RX_F_P 13 43
R631 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_RX_F_N 13 43
R632 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_D_TX_P 13 43
R633 USB3_TX_CONN	USB3_PHV	USB3	USB3_EXT_D_TX_N 13 43
R634 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_TX_F_P 43
R635 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_TX_F_N 43
R636 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_TX_C_P 43
R637 USB3_PHV	USB3_PHV	USB3	USB3_EXT_D_TX_C_N 43
R638 USB2_CONN	USB2_PHV	USB2	USB_EXT_D_9_P 13 43
R639 USB2_CONN	USB2_PHV	USB2	USB_EXT_D_9_N 13 43
R640 USB2_PHV	USB2_PHV	USB2	USB2_EXT_D_P 43
R641 USB2_PHV	USB2_PHV	USB2	USB2_EXT_D_N 43
<b>Camera (J3510)</b>			
R642 USB2_CONN_TNT	USB2_PHV	USB2	USB_CAMERA_P 13 38
R643 USB2_CONN_TNT	USB2_PHV	USB2	USB_CAMERA_N 13 38
<b>PCH USB Compensation</b>			
R644 PCH_5SS	COMP_PCH	PCH_USB_RBIA5	13

Electrical Constraint Set	Physical	Spacing
USB2_MIXED_BT	USB2_EHV	USB2
USB2_MIXED_BT	USB2_EHV	USB2
USB2_MIXED_BT	USB2_EHV	USB2
USB2_MIXED_BT	USB2_EHV	USB2

Electrical Contact Set	Physical	Spacing
Ethernet		
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF
ENET_MDI	ENET_DIFF_PHY	ENET_TRANS
ENET_MDI	ENET_DIFF_PHY	ENET_TRANS
		ENET_TRANS
		ENET_TRANS
		ENET_TRANS
		ENET_TRANS
		ENET_TRANS
	ENET_COMP_PHY	COMP_ENET
SD		
SD_DATA	SD_PHY	SD
	SD_PHY	SD
SD_CMD	SD_PHY	SD
	SD_PHY	SD
	SD_PHY	SD
SD_CLK	SD_PHY	SD
	SD_PHY	SD
	SD_PHY	SD
	SD_PHY	SD
	SD_PHY	SD
CIV SPI		
	CTV_SPI	SPI
	CTV_SPI	SPI
	CTV_SPI	SPI
	CTV_SPI	SPI

Electrical Constraint Set		Physical	Spacing
REQ1	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ2	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ3	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ4	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ5			
REQ6		SPI_50S	SPI
REQ7		SPI_50S	SPI
REQ8		SPT_50S	SET
REQ9		SPT_50S	SET
REQ10		SPT_50S	SPI
REQ11		SPT_50S	SPI
REQ12		SPT_50S	SPI
REQ13		SPT_50S	SPI
REQ14		SPT_50S	SPI
REQ15		SMB_PHY	SMB
REQ16		SMB_PHY	SMB

Electrical Constraint Set		Physical	Spacing
REQ1	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ2	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ3	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ4	SMTA_DP	SMTA_DIFF_PHY	SMTA_DIFF
REQ5			
REQ6		SPI_50S	SPI
REQ7		SPI_50S	SPI
REQ8		SPT_50S	SET
REQ9		SPT_50S	SET
REQ10		SPT_50S	SPI
REQ11		SPT_50S	SPI
REQ12		SPT_50S	SPI
REQ13		SPT_50S	SPI
REQ14		SPT_50S	SPI
REQ15		SMB_PHY	SMB
REQ16		SMB_PHY	SMB

SYNCH MASTER=J16 MLB		SYNCH DATE=12/03/2012	
PAGE TITLE			
USB/Ethernet/SD Constraints			
 Apple Inc.		DRAWING NUMBER	051-0164
		SIZE	D
		REVISION	12.4.0
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## D

## C

B

## A

1

## C

## B

A

## D

B

## Constraints

Constraints			
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO


CPU Core			
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~~SMBus~~

100

Temperature Sense

SYNC MASTER=J16 NICK		SYNC DATE=01/10/2013	
PAGE TITLE			
SMBus/Sensor Constraints		DRAWING NUMBER	
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CPU VCC Phases																																																																																																																																																																																																																																																																																																																																																																															
<table><tr><th>Electrical Constraint Set</th><th>Physical</th><th>Spacing</th><th>Voltage</th><th>DIDT</th><th>NO_TEST</th><th></th><th></th></tr><tr><td colspan="8">Input Bus</td></tr><tr><td>1397</td><td>POWER</td><td>POWER</td><td>1.2V</td><td></td><td></td><td>PP12V_S0_CPUVCC_FLT</td><td>61 62</td></tr><tr><td>1398</td><td>POWER</td><td>POWER</td><td>5V</td><td></td><td></td><td>REG_VCC_U7000</td><td>61</td></tr><tr><td colspan="8">Local Ground</td></tr><tr><td>1399</td><td>GND</td><td>GND</td><td>0V</td><td></td><td></td><td>AGND_CPU</td><td>61 62 71</td></tr><tr><td colspan="8">Phase 1</td></tr><tr><td>1400</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_THWN_1</td><td>62</td></tr><tr><td>1401</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_1</td><td>61 62</td></tr><tr><td>1402</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_1_R</td><td>61</td></tr><tr><td>1403</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC_1</td><td>62</td></tr><tr><td>1404</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC1</td><td>62</td></tr><tr><td>1405</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_BOOT_CPUVCC_1</td><td>62</td></tr><tr><td>1406</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>TRUE</td><td>REG_BOOT_CPUVCC_1_RC</td><td>62</td></tr><tr><td>1407</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_SNUBBER_CPUVCC_1</td><td>62</td></tr><tr><td>1408</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td></td><td>PPCPUVCC_S0_SENSE_1</td><td>62</td></tr><tr><td>1409</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_1_P</td><td>61 62</td></tr><tr><td>1410</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_1_N</td><td>62</td></tr><tr><td>1411</td><td></td><td></td><td></td><td></td><td></td><td>REG_ISENVC_1_NR</td><td>61 62</td></tr><tr><td colspan="8">Phase 2</td></tr><tr><td>1412</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_THWN_2</td><td>62</td></tr><tr><td>1413</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_2</td><td>61 62</td></tr><tr><td>1414</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_2_R</td><td>61</td></tr><tr><td>1415</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC_2</td><td>62</td></tr><tr><td>1416</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC2</td><td>62</td></tr><tr><td>1417</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_BOOT_CPUVCC_2</td><td>62</td></tr><tr><td>1418</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>TRUE</td><td>REG_BOOT_CPUVCC_2_RC</td><td>62</td></tr><tr><td>1419</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_SNUBBER_CPUVCC_2</td><td>62</td></tr><tr><td>1420</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td></td><td>PPCPUVCC_S0_SENSE_2</td><td>62</td></tr><tr><td>1421</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_2_P</td><td>61 62</td></tr><tr><td>1422</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_2_N</td><td>62</td></tr><tr><td>1423</td><td></td><td></td><td></td><td></td><td></td><td>REG_ISENVC_2_NR</td><td>61 62</td></tr><tr><td colspan="8">Phase 3</td></tr><tr><td>1424</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_THWN_3</td><td>62</td></tr><tr><td>1425</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_3</td><td>61 62</td></tr><tr><td>1426</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_PWM_CPUVCC_3_R</td><td>61</td></tr><tr><td>1427</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC_3</td><td>62</td></tr><tr><td>1428</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_PHASE_CPUVCC3</td><td>62</td></tr><tr><td>1429</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_BOOT_CPUVCC_3</td><td>62</td></tr><tr><td>1430</td><td>VR_DIDT_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td>TRUE</td><td>REG_BOOT_CPUVCC_3_RC</td><td>62</td></tr><tr><td>1431</td><td>VR_CTL_PHY</td><td>VR_SWITCH</td><td>1.2V</td><td>TRUE</td><td></td><td>REG_SNUBBER_CPUVCC_3</td><td>62</td></tr><tr><td>1432</td><td>POWER</td><td>POWER</td><td>1.8V</td><td></td><td></td><td>PPCPUVCC_S0_SENSE_3</td><td>62</td></tr><tr><td>1433</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_3_P</td><td>61 62</td></tr><tr><td>1434</td><td>ISNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>REG_ISENVC_3_N</td><td>62</td></tr><tr><td>1435</td><td></td><td></td><td></td><td></td><td></td><td>REG_ISENVC_3_NR</td><td>61 62</td></tr></table>								Electrical Constraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST			Input Bus								1397	POWER	POWER	1.2V			PP12V_S0_CPUVCC_FLT	61 62	1398	POWER	POWER	5V			REG_VCC_U7000	61	Local Ground								1399	GND	GND	0V			AGND_CPU	61 62 71	Phase 1								1400	VR_CTL_PHY	VR_CTL				REG_THWN_1	62	1401	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1	61 62	1402	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1_R	61	1403	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC_1	62	1404	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC1	62	1405	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_BOOT_CPUVCC_1	62	1406	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	TRUE	REG_BOOT_CPUVCC_1_RC	62	1407	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_SNUBBER_CPUVCC_1	62	1408	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1	62	1409	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_1_P	61 62	1410	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_1_N	62	1411						REG_ISENVC_1_NR	61 62	Phase 2								1412	VR_CTL_PHY	VR_CTL				REG_THWN_2	62	1413	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2	61 62	1414	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2_R	61	1415	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC_2	62	1416	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC2	62	1417	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_BOOT_CPUVCC_2	62	1418	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	TRUE	REG_BOOT_CPUVCC_2_RC	62	1419	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_SNUBBER_CPUVCC_2	62	1420	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2	62	1421	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_2_P	61 62	1422	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_2_N	62	1423						REG_ISENVC_2_NR	61 62	Phase 3								1424	VR_CTL_PHY	VR_CTL				REG_THWN_3	62	1425	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3	61 62	1426	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3_R	61	1427	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC_3	62	1428	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_PHASE_CPUVCC3	62	1429	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE		REG_BOOT_CPUVCC_3	62	1430	VR_DIDT_PHY	VR_SWITCH	1.2V	TRUE	TRUE	REG_BOOT_CPUVCC_3_RC	62	1431	VR_CTL_PHY	VR_SWITCH	1.2V	TRUE		REG_SNUBBER_CPUVCC_3	62	1432	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_3	62	1433	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_3_P	61 62	1434	ISNS_CPU_CORE	SNS_DIFF_PHY				REG_ISENVC_3_N	62	1435						REG_ISENVC_3_NR	61 62
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colspan="8">ISL6372</td></tr><tr><td>1436</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_DVC</td><td>61</td></tr><tr><td>1437</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_DVC_RC</td><td>61</td></tr><tr><td>1438</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_FB_RC_2</td><td>61</td></tr><tr><td>1439</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_COMP</td><td>61</td></tr><tr><td>1440</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_COMP_RC</td><td>61</td></tr><tr><td>1441</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_FB</td><td>61</td></tr><tr><td>1442</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_FB_RC</td><td>61</td></tr><tr><td>1443</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_FB_R_1</td><td>61</td></tr><tr><td>1444</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_FB_R_2</td><td>61</td></tr><tr><td>1445</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_PSICOMP_RC</td><td>61</td></tr><tr><td>1446</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_PSICOMP</td><td>61</td></tr><tr><td>1447</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_HFCOMP</td><td>61</td></tr><tr><td>1448</td><td>VSNS_CPU_CORE</td><td>SNS_DIFF_PHY</td><td></td><td></td><td></td><td>CPU_VCCSENSE_P</td><td>6 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61</td></tr><tr><td>1458</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>CPUVCC_IMON_R</td><td>61</td></tr><tr><td>1459</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_TM</td><td>61</td></tr><tr><td>1460</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_IMX</td><td>61</td></tr><tr><td>1461</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_NPSI</td><td>61</td></tr><tr><td>1462</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_FDVID</td><td>61</td></tr><tr><td>1463</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_TMX</td><td>61</td></tr><tr><td>1464</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_MEMVRSEL</td><td>61</td></tr><tr><td>1465</td><td>VR_CTL_PHY</td><td>VR_CTL</td><td></td><td></td><td></td><td>REG_CPUVCC_RSET</td><td>61</td></tr><tr><td>1466</td><td>CPU_VIDSCLK</td><td>VR_VID_PHY</td><td>VR_VID</td><td></td><td></td><td>CPU_VIDSCLK</td><td>6 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Set	Physical	Spacing	Voltage	DIDT	NO_TEST			ISL6372								1436	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DVC	61	1437	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC	61	1438	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2	61	1439	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP	61	1440	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC	61	1441	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB	61	1442	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC	61	1443	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1	61	1444	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2	61	1445	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC	61	1446	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP	61	1447	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP	61	1448	VSNS_CPU_CORE	SNS_DIFF_PHY				CPU_VCCSENSE_P	6 61	1449	VSNS_CPU_CORE	SNS_DIFF_PHY				CPU_VCCSENSE_N	9 61	1450		SNS_DIFF_PHY				CPU_VCCSENSE_R_P	61	1451		SNS_DIFF_PHY				CPU_VCCSENSE_R_N	61	1452		SNS_DIFF_PHY				SNS_VCC_XW_P	61	1453		SNS_DIFF_PHY				SNS_VCC_XW_N	61	1454						REG_CPUVCC_VSEN	61	1455						REG_CPUVCC_RGND	61	1456						REG_CPUVCC_VIN	61	1457	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON	48 61	1458	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R	61	1459	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM	61	1460	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX	61	1461	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI	61	1462	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID	61	1463	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX	61	1464	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL	61	1465	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET	61	1466	CPU_VIDSCLK	VR_VID_PHY	VR_VID			CPU_VIDSCLK	6 61	1467	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	6	1468	CPU_VIDALERT_L	VR_VID_PHY	VR_VID			CPU_VIDALERT_L	6 61	1469	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	6	1470	CPU_VIDSOUT	VR_VID_PHY	VR_VID			CPU_VIDSOUT	6 61	1471	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	6	Output Bus								1472	POWER	POWER	1.8V			PPCPUVCC_S0_CPU	70																																								
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1437	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC	61																																																																																																																																																																																																																																																																																																																																																																								
1438	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2	61																																																																																																																																																																																																																																																																																																																																																																								
1439	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP	61																																																																																																																																																																																																																																																																																																																																																																								
1440	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC	61																																																																																																																																																																																																																																																																																																																																																																								
1441	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB	61																																																																																																																																																																																																																																																																																																																																																																								
1442	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC	61																																																																																																																																																																																																																																																																																																																																																																								
1443	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1	61																																																																																																																																																																																																																																																																																																																																																																								
1444	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2	61																																																																																																																																																																																																																																																																																																																																																																								
1445	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC	61																																																																																																																																																																																																																																																																																																																																																																								
1446	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP	61																																																																																																																																																																																																																																																																																																																																																																								
1447	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP	61																																																																																																																																																																																																																																																																																																																																																																								
1448	VSNS_CPU_CORE	SNS_DIFF_PHY				CPU_VCCSENSE_P	6 61																																																																																																																																																																																																																																																																																																																																																																								
1449	VSNS_CPU_CORE	SNS_DIFF_PHY				CPU_VCCSENSE_N	9 61																																																																																																																																																																																																																																																																																																																																																																								
1450		SNS_DIFF_PHY				CPU_VCCSENSE_R_P	61																																																																																																																																																																																																																																																																																																																																																																								
1451		SNS_DIFF_PHY				CPU_VCCSENSE_R_N	61																																																																																																																																																																																																																																																																																																																																																																								
1452		SNS_DIFF_PHY				SNS_VCC_XW_P	61																																																																																																																																																																																																																																																																																																																																																																								
1453		SNS_DIFF_PHY				SNS_VCC_XW_N	61																																																																																																																																																																																																																																																																																																																																																																								
1454						REG_CPUVCC_VSEN	61																																																																																																																																																																																																																																																																																																																																																																								
1455						REG_CPUVCC_RGND	61																																																																																																																																																																																																																																																																																																																																																																								
1456						REG_CPUVCC_VIN	61																																																																																																																																																																																																																																																																																																																																																																								
1457	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON	48 61																																																																																																																																																																																																																																																																																																																																																																								
1458	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R	61																																																																																																																																																																																																																																																																																																																																																																								
1459	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM	61																																																																																																																																																																																																																																																																																																																																																																								
1460	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX	61																																																																																																																																																																																																																																																																																																																																																																								
1461	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI	61																																																																																																																																																																																																																																																																																																																																																																								
1462	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID	61																																																																																																																																																																																																																																																																																																																																																																								
1463	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX	61																																																																																																																																																																																																																																																																																																																																																																								
1464	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL	61																																																																																																																																																																																																																																																																																																																																																																								
1465	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET	61																																																																																																																																																																																																																																																																																																																																																																								
1466	CPU_VIDSCLK	VR_VID_PHY	VR_VID			CPU_VIDSCLK	6 61																																																																																																																																																																																																																																																																																																																																																																								
1467	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	6																																																																																																																																																																																																																																																																																																																																																																								
1468	CPU_VIDALERT_L	VR_VID_PHY	VR_VID			CPU_VIDALERT_L	6 61																																																																																																																																																																																																																																																																																																																																																																								
1469	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	6																																																																																																																																																																																																																																																																																																																																																																								
1470	CPU_VIDSOUT	VR_VID_PHY	VR_VID			CPU_VIDSOUT	6 61																																																																																																																																																																																																																																																																																																																																																																								
1471	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	6																																																																																																																																																																																																																																																																																																																																																																								
Output Bus																																																																																																																																																																																																																																																																																																																																																																															
1472	POWER	POWER	1.8V			PPCPUVCC_S0_CPU	70																																																																																																																																																																																																																																																																																																																																																																								
8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																								



## Thunderbolt

## Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

### Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

## DisplayPort

## DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

### DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.

Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

## TBT IC Net Properties

Electrical Constraint Set	Physical	Spacing			
H590	DP 85D	DISPLAYPORT	DP TBTSNKO ML C P<3...0>	26 71	
H591	DP 85D	DISPLAYPORT	DP TBTSNKO ML C N<3...0>	26 71	
H592	DP TBTSNKO ML	DP 85D	DISPLAYPORT	DP TBTSNKO ML P<3...0>	26
H593	DP TBTSNKO ML	DP 85D	DISPLAYPORT	DP TBTSNKO ML N<3...0>	26
H594	DP 85D	DISPLAYPORT	DP TBTSNKO AUXCH C P	26 71	
H595	DP 85D	DISPLAYPORT	DP TBTSNKO AUXCH C N	26	
H596	DP TBTSNKO AUX	DP 85D	DISPLAYPORT	DP TBTSNKO AUXCH P	26
H597	DP TBTSNKO AUX	DP 85D	DISPLAYPORT	DP TBTSNKO AUXCH N	26
H598		DP 85D	DISPLAYPORT	DP TBTSNKL ML C P<3...0>	26 71
H599		DP 85D	DISPLAYPORT	DP TBTSNKL ML C N<3...0>	26 71
H600	DP TBTSNKL ML	DP 85D	DISPLAYPORT	DP TBTSNKL ML P<3...0>	26
H601	DP TBTSNKL ML	DP 85D	DISPLAYPORT	DP TBTSNKL ML N<3...0>	26
H602	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH C P	26 71	
H603	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH C N	26 71	
H604	DP TBTSNKL AUX	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H605	DP TBTSNKL AUX	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H606		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H607		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H608	DP TBTSNKL AUX	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H609	DP TBTSNKL AUX	DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H610		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H611		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H612		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H613		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H614		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H615		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H616		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H617		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H618		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H619		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H620		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H621		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H622		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H623		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H624		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H625		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H626		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H627		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H628		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H629		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H630		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H631		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H632		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H633		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H634		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H635		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H636		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H637		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H638		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H639		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H640		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H641		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H642		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H643		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H644		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H645		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H646		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H647		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H648		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H649		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H650		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H651		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H652		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H653		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H654		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H655		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H656		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H657		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H658		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H659		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H660		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H661		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H662		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H663		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H664		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H665		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H666		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H667		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H668		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H669		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H670		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H671		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H672		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H673		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H674		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H675		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H676		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H677		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H678		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H679		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H680		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H681		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H682		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H683		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H684		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H685		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H686		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H687		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H688		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H689		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H690		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
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H692		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H693		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
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H700		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
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H705		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
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H711		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H712		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H713		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H714		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H715		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H716		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H717		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H718		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H719		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H720		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H721		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H722		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H723		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H724		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H725		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H726		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H727		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H728		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H729		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H730		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H731		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H732		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H733		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H734		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H735		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H736		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
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H738		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H739		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H740		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H741		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H742		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H743		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H744		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H745		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H746		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H747		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H748		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H749		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H750		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H751		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H752		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H753		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H754		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H755		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H756		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H757		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H758		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H759		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H760		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H761		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H762		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H763		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H764		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H765		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H766		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H767		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H768		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H769		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H770		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H771		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H772		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H773		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H774		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H775		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H776		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H777		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H778		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H779		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H780		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H781		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H782		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H783		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H784		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H785		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H786		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H787		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H788		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H789		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H790		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H791		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H792		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H793		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H794		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H795		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H796		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H797		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H798		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H799		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H800		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H801		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H802		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H803		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H804		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H805		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H806		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H807		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H808		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H809		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H810		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H811		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H812		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H813		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H814		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H815		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H816		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H817		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H818		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	26
H819		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH N	26
H820		DP 85D	DISPLAYPORT	DP TBTSNKL AUXCH P	

\*: Only used on hosts supporting T29 video-in

## DisplayPort

Electrical Constraint Set	Physical	Spacing	
Graphics Source			
R549	DP_INTENL_EG_ML_MUX	DP_85D	DISPLAYPORT DP_INT ML P<1..0> 41
R549	DP_INTENL_EG_ML_MUX	DP_85D	DISPLAYPORT DP_INT ML N<1..0> 41 71
R549	DP_INTENL_EG_AUX_MUX	DP_85D	DISPLAYPORT DP_INT_AUX_P 41 71
R549	DP_INTENL_EG_AUX_MUX	DP_85D	DISPLAYPORT DP_INT_AUX_N 41 71
R549		DP_85D	DISPLAYPORT DP_INT_AUX_C_P 41
R549		DP_85D	DISPLAYPORT DP_INT_AUX_C_N 41
Internal Panel			
R590		DP_85D	DISPLAYPORT DP_INTPNL ML_C_P<3..0> 41
R590		DP_85D	DISPLAYPORT DP_INTPNL ML_C_N<3..0> 41
R590	DP_INTENL_ML_CONN	DP_85D	DISPLAYPORT DP_INTPNL ML_P<3..0> 41 41
R590	DP_INTENL_ML_CONN	DP_85D	DISPLAYPORT DP_INTPNL ML_N<3..0> 41 41
R590	DP_INTENL_AUX_CONN	DP_85D	DISPLAYPORT DP_INTPNL_AUX_P 41 41
R590	DP_INTENL_AUX_CONN	DP_85D	DISPLAYPORT DP_INTPNL_AUX_N 41 41
Internal DP SPDIF			
R589		HDA	DP_INT_SPDIF_AUDIO 40 52

### TBT/DP Net Properties

Electrical Constraint Set		Physical	Spacing	
Port A				
16001	TBT A R2D1	TBTDP_90D	TBTDP	TBT A R2D C P<1>
16002	TBT A R2D1	TBTDP_90D	TBTDP	TBT A R2D C N<1>
16003	TBT A R2D0	TBTDP_90D	TBTDP	TBT A R2D C P<0>
16004	TBT A R2D0	TBTDP_90D	TBTDP	TBT A R2D C N<0>
16005		TBTDP_90D	TBTDP	TBT A R2D P<1..0>
16006		TBTDP_90D	TBTDP	TBT A R2D N<1..0>
16007	DP_TBTPA_ML1	DP_85D	DISLAYEPORT	DP TBTPA ML C P<1>
16008	DP_TBTPA_ML1	DP_85D	DISLAYEPORT	DP TBTPA ML C N<1>
16009	DP_TBTPA_ML3	DP_85D	DISLAYEPORT	DP TBTPA ML C P<3>
16010	DP_TBTPA_ML3	DP_85D	DISLAYEPORT	DP TBTPA ML C N<3>
16011		DP_85D	DISLAYEPORT	DP TBTPA ML P<1>
16012		DP_85D	DISLAYEPORT	DP TBTPA ML N<1>
16013		DP_85D	DISLAYEPORT	DP TBTPA ML P<3>
16014		DP_85D	DISLAYEPORT	DP TBTPA ML N<3>
16015	DP_A_LSX	DP_85D	DISLAYEPORT	DP A LSX ML P<1>
16016	DP_A_LSX	DP_85D	DISLAYEPORT	DP A LSX ML N<1>
16017		TBTDP_90D	TBTDP	TBT A D2R C P<1..0>
16018		TBTDP_90D	TBTDP	TBT A D2R C N<1..0>
16019	TBT A D2R1	TBTDP_90D	TBTDP	TBT A D2R P<1>
16020	TBT A D2R1	TBTDP_90D	TBTDP	TBT A D2R N<1>
16021	TBT A D2R0	TBTDP_90D	TBTDP	TBT A D2R P<0>
16022	TBT A D2R0	TBTDP_90D	TBTDP	TBT A D2R N<0>
16023	TBT A AUXCH	DP_85D	DISLAYEPORT	DP TBTPA AUXCH C P
16024	TBT A AUXCH	DP_85D	DISLAYEPORT	DP TBTPA AUXCH C N
16025		DP_85D	DISLAYEPORT	DP TBTPA AUXCH P
16026		DP_85D	DISLAYEPORT	DP TBTPA AUXCH N
16027	DP_A_AUXCH_DDC	DP_85D	DISLAYEPORT	DP A AUXCH DDC P
16028	DP_A_AUXCH_DDC	DP_85D	DISLAYEPORT	DP A AUXCH DDC N
16029		TBTDP_90D	TBTDP	TBT A D2R1 AUXDDC P
16030		TBTDP_90D	TBTDP	TBT A D2R1 AUXDDC N
Port B				
16031	TBT B R2D1	TBTDP_90D	TBTDP	TBT B R2D C P<1>
16032	TBT B R2D1	TBTDP_90D	TBTDP	TBT B R2D C N<1>
16033	TBT B R2D0	TBTDP_90D	TBTDP	TBT B R2D C P<0>
16034	TBT B R2D0	TBTDP_90D	TBTDP	TBT B R2D C N<0>
16035		TBTDP_90D	TBTDP	TBT B R2D P<1..0>
16036		TBTDP_90D	TBTDP	TBT B R2D N<1..0>
16037	DP_TBTPB_ML1	DP_85D	DISLAYEPORT	DP TBTPB ML C P<1>
16038	DP_TBTPB_ML1	DP_85D	DISLAYEPORT	DP TBTPB ML C N<1>
16039	DP_TBTPB_ML3	DP_85D	DISLAYEPORT	DP TBTPB ML C P<3>
16040	DP_TBTPB_ML3	DP_85D	DISLAYEPORT	DP TBTPB ML C N<3>
16041		DP_85D	DISLAYEPORT	DP TBTPB ML P<1>
16042		DP_85D	DISLAYEPORT	DP TBTPB ML N<1>
16043		DP_85D	DISLAYEPORT	DP TBTPB ML P<3>
16044		DP_85D	DISLAYEPORT	DP TBTPB ML N<3>
16045	DP_B_LSX	DP_85D	DISLAYEPORT	DP B LSX ML P<1>
16046	DP_B_LSX	DP_85D	DISLAYEPORT	DP B LSX ML N<1>
16047		TBTDP_90D	TBTDP	TBT B D2R C P<1..0>
16048		TBTDP_90D	TBTDP	TBT B D2R C N<1..0>
16049	TBT B D2R1	TBTDP_90D	TBTDP	TBT B D2R P<1>
16050	TBT B D2R1	TBTDP_90D	TBTDP	TBT B D2R N<1>
16051	TBT B D2R0	TBTDP_90D	TBTDP	TBT B D2R P<0>
16052	TBT B D2R0	TBTDP_90D	TBTDP	TBT B D2R N<0>
16053	TBT B AUXCH	DP_85D	DISLAYEPORT	DP TBTPB AUXCH C P
16054	TBT B AUXCH	DP_85D	DISLAYEPORT	DP TBTPB AUXCH C N
16055		DP_85D	DISLAYEPORT	DP TBTPB AUXCH P
16056		DP_85D	DISLAYEPORT	DP TBTPB AUXCH N
16057	DP_B_AUXCH_DDC	DP_85D	DISLAYEPORT	DP B AUXCH DDC P
16058	DP_B_AUXCH_DDC	DP_85D	DISLAYEPORT	DP B AUXCH DDC N
16059		TBTDP_90D	TBTDP	TBT B D2R1 AUXDDC P
16060		TBTDP_90D	TBTDP	TBT B D2R1 AUXDDC N

## Backlight Controller

## BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

## Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

### BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

## BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	= 3 : 1_SPACING	?

## Constraints

## BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

## BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

Physical	Spacing	Voltage	DITD	NO_TEST
Input Bus				
POWER	POWER	12V		PP12V_BKLT_SNS
POWER	POWER	12V		PP12V_BKLT_FUSED
POWER	POWER	12V		PP12V_S0_BKLT_FILT
POWER	POWER	12V		PP12V_S0_BKLT_PWR
POWER	POWER	12V		PP12V_S0_BKLT_PWR_R
POWER	POWER	5V		PP5V_S0_BKLT_R
POWER	POWER	3.3V		PP3V3_S0_BKLT_VDDIO_R
Local Ground				
BLC_CTL_PHV	BLC_PHASE	0V		PGND_BKLT
BLC_CTL_PHV	BLC_PHASE	0V		DGND_BKLT
BLC_CTL_PHV	BLC_PHASE	0V		LGND_BKLT
Backlight				
POWER_BLC	BLC_PHASE	80V	TRUE	BKLT_PHASE
BLC_CTL_PHV	BLC_PHASE	80V	TRUE	BKLT_GATE
BLC_CTL_PHV	BLC_PHASE	80V	TRUE	BKLT_GATE_R
BLC_CTL_PHV	BLC_PHASE	80V	TRUE	BKLT_SNUBBER
BLC_CTL_PHV	BLC_PHASE	12V	TRUE	BKLT_SW_R
BLC_CTL_PHV	BLC_CTL			BKLT_ISET
BLC_CTL_PHV	BLC_CTL			BKLT_FLT
BLC_CTL_PHV	BLC_CTL			BKLT_FLT_RC
SNS_DIFF_PHV	SENSE			BKLT_SW_P
SNS_DIFF_PHV	SENSE			BKLT_SW_N
SNS_DIFF_PHV	SENSE			BKLT_FB
BLC_HV		67V		BKLT_FB_XW
BLC_HV		67V		BKLT_FB_R
POWER_BLC_RET	BLC_CTL			BKLT_ISEN1
POWER_BLC_RET	BLC_CTL			BKLT_ISEN2
POWER_BLC_RET	BLC_CTL			BKLT_ISEN3
POWER_BLC_RET	BLC_CTL			BKLT_ISEN4
POWER_BLC_RET	BLC_CTL			BKLT_ISEN5
POWER_BLC_RET	BLC_CTL			BKLT_ISEN6
POWER_BLC_RET	BLC_HV			BKLT_ISEN1_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN2_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN3_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN4_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN5_R
POWER_BLC_RET	BLC_HV			BKLT_ISEN6_R
POWER_BLC_RET	BLC_HV			LED_RETURN_1
POWER_BLC_RET	BLC_HV			LED_RETURN_2
POWER_BLC_RET	BLC_HV			LED_RETURN_3
POWER_BLC_RET	BLC_HV			LED_RETURN_4
POWER_BLC_RET	BLC_HV			LED_RETURN_5
POWER_BLC_RET	BLC_HV			LED_RETURN_6
Output Bus				
POWER_BLC	BLC_HV	67V		BKLT_BOOST
POWER_BLC	BLC_HV	67V		BKLT_BOOST_1
POWER_BLC	BLC_HV	67V		BKLT_BOOST_2

Cello Miscellaneous

Electrical Constraint Set	Physical	Spacing	
SPI			
	SMB_PHY	SMB	BKLT_SCL 60
	SMB_PHY	SMB	BKLT_SDA 60